



# Radio Frequency Micro Electro Mechanical Systems- An Overview

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## Abstract

This paper reviews the design and development of different building blocks of RF MEMS sub-systems. The blocks include switches, tunable capacitors, integrated inductors, filters, reconfigurable circuits, phase shifters and antennas. Starting with the details of a general micromachining process, a behavioral analysis of RF MEMS components and design challenges with present state-of-the-art are discussed. Different fabrication processes are outlined and discussed. The functional behaviors of different RF MEMS components are experimentally investigated over certain frequency bands of interest and validated through system level simulation. Finally, a low cost packaging scheme has been presented.

## 1. Introduction

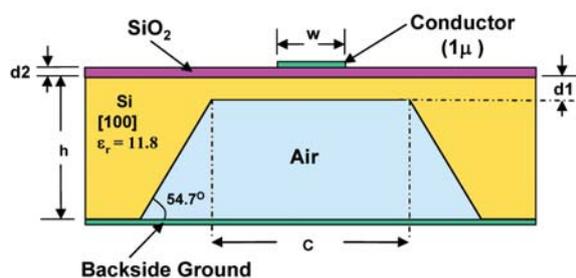
Radio frequency micro-electro-mechanical-systems (RF MEMS) is an enabling technology for wireless communication and millimetre-wave systems. The motivation for the fabrication of high frequency circuits using MEMS technology is due to high levels of functionality with low power consumption, precise dimensions and electrically activated moving parts. There is considerable interest in developing reconfigurable and tunable integrated RF MEMS front ends using high dielectric constant substrates such as Si, alumina and GaAs [Mowler *et al.*, 2005, Vähä-Heikkilä *et al.*, 2005, Malmquist *et al.*, 2006, Schaffoer *et al.*, 2000, Brown *et al.*, 1998]. In addition, due to the high dielectric constant of the substrate, there is a possibility of excitation of surface waves. These problems can be overcome by introducing a small air gap between the dielectric substrate and the ground plane as shown in Figure 1. The air gap can be created easily using bulk micromachining technique. The advantages of creating a small air

gap beneath the signal conductor are: (a) a lower effective dielectric constant, hence wider circuit dimensions, (b) ease of fabrication and relaxed dimensional tolerances, (c) lower attenuation, (d) enhanced radiation efficiency in the case of antennas and (e) elimination of surface waves. Using the micromachined lines, it is possible to design and develop high performance passive circuits and printed micromachined antennas at microwave and millimetre wave frequencies. An RF MEMS switch is another important component that finds application as a discrete device and in integrated circuits. The design, modelling and development of a variety of RF MEMS switches on Quartz, Si and GaAs substrates are reported in the literature [Rizk *et al.*, 2003, Lee *et al.*, 2004, Zheng *et al.*, 2005].

Due to their superior performance over solid-state switches, they are widely used in reconfigurable systems, tuning circuits and phase-shifter applications.

RF MEMS devices can be fabricated using two different micromachining processes: Bulk

micromachining and Surface micromachining. Bulk micromachining defines structures by selectively etching inside a substrate. Whereas surface micromachining creates structures on top of a substrate, bulk micromachining produces structures inside a substrate. Bulk micromachining starts with a silicon wafer or other substrates that are selectively etched, using photolithography to transfer a pattern from a mask to the surface. Surface micromachining builds microstructures by the deposition and etching of different structural layers on top of the substrate.



**Figure 1** Cross-section of a micromachined microstrip line.

RF MEMS components that are currently under development in laboratories and industries include switches, tunable capacitors, high quality factor ( $Q$ ) micromachined inductors, filters, reconfigurable circuits, phase shifters and antennas. Among them, a lot of work has been done in the field of modelling of RF MEMS switches in order to use them easily within circuit simulators. A rigorous distributed-lumped CLR model has been provided by Muldavin [Muldavin *et al.*, 2000]. In their work, capacitive MEMS and DC-contact switches are represented by a capacitor-inductor-resistor (CLR) series combination. The tunable capacitors, inductors and filters are finding growing applications in reconfigurable integrated circuit like voltage controlled oscillators, power amplifier and software programmable RF front-end and digital receivers. Radio frequency micro-electromechanical system (RFMEMS)-based phase shifter is typically used for broadband applications with low loss for RF transmission, improved power handling capability, and compatibility with traditional MMIC circuits. These phase shifters offer light weight and low costs compared to ferrite-based phase shifters [Rebeiz *et al.*, 2002]. The major parameters that define the

performance of RF and microwave phase shifters are centre frequency, bandwidth (BW), total phase variance ( $\Delta\phi$ ), insertion loss (IL), switching speed, power handling (P), phase setting accuracy and resolution, input/output matching (VSWR) or return loss (RL), and harmonics level [Lee *et al.*, 2004]. Another important circuit element is the MEMS antenna. One can either develop stand alone high performance antennas or develop reconfigurable antennas. There are various methods to achieve reconfigurability in terms of frequency, bandwidth, polarization and the radiation pattern of the antennas. A popular method is to change the shape of the effective radiating structure to alter the radiation pattern or the frequency of operation. In another method, an antenna can actuate mechanically, thereby changing the orientation of the antenna with respect to the substrate or another radiating structure. Impedance modification of the antenna is also another method to change the resonant frequency of the radiating antenna. To reconfigure the antenna in a dynamic manner, tunable components such as RF MEMS switches and varactors are used. As compared to conventional microwave components (such as P-i-N diode switches, MESFET, Varactor diode etc.), RF MEMS technology enables the production of dynamically-tuned reconfigurable structures more efficiently in terms of low insertion losses, low power consumption, high linearity and high performance. Moreover, the monolithic fabrication of the antenna together with these tunable components reduces the power losses and parasitic effects compared to the integration of discrete components. RF MEMS components can also be used to realize MCM (multi-chip-module) and SOC (system-on-chip) with the high-density package that leads to a reduction of the size and weight of the RF components [Skolnik *et al.*, 2005, Maciel *et al.*, 2007].

Our work focuses on developing different RF MEMS components with minimum loss and good reliability at certain frequency-bands of interest. Different surface- micromachining and bulk-micromachining processes have been used to develop RF MEMS components. To understand the effect of release, damping and electromechanical behaviour for different MEMS devices with various structural modifications, the polyMUMPs process

plays a very important role in the first phase of the study. The final phase deals with a RF compatible process with different layer-by-layer modification based on device functionality.

The objective of this paper is to review our research work on RF MEMS during the past decade. The organization of the paper is as follows. The RF MEMS switch has been discussed with different fabrication process flows in Section 2. MEMS varactors, inductors, phase shifters, filters, reconfigurable circuits and antennas have been discussed and presented in subsequent sections.

## 2. RF switch

RF MEMS switches offer many advantages over contemporary solid-state switches in terms of low loss, high isolation, low power consumption and high linearity. The disadvantages of MEMS switches are low switching speed ( $\mu\text{s}$  range) and high actuation voltage. In many telecommunication applications, such as low-loss high isolation RF switching, these drawbacks do not pose any major problem. Several methods are reported in the literature for the design of high-isolation switches. MEMS switches are surface-micro-machined devices that use mechanical movement to achieve a short circuit or an open circuit in the RF transmission-line. In a shunt switch, a metal beam (membrane) is placed in shunt between the transmission line (t-line) and the ground. With no applied bias voltage, the switch is in the up-state, and when biased, the metal beam falls down and shorts the t-line with the ground. MEMS RF switches are classified according to the type of contact as metal-to-metal contact switches and capacitive switches. In the metal-to-metal contact switch, there is direct contact between the t-line and the metal beam. The resistive contact switch permits operation down to DC. The frequency of operation reported for these switches is DC-110 GHz. In the capacitive switches, the contact is via an insulating dielectric layer. The blocking capacitor stops the low frequency signals passing through. The frequency of operation reported for these switches is 10-120 GHz.

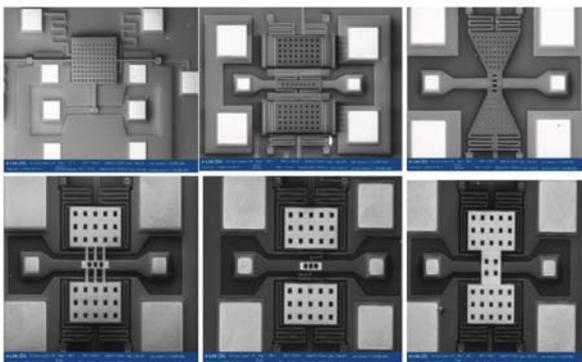
The Raytheon shunt capacitive switch, also known as the Texas Instruments switch, is a simple switch that was developed by Chuck Goldsmith and his co-workers in 1995–2000 [Shen *et al.*, 2000].

The Raytheon switch is very similar to the standard MEMS capacitive switch, and has undergone three main iterations to result in an outstanding MEMS capacitive switch. This switch has been extensively used in X-band and K-band phase shifters, switched capacitor banks and tunable filters, and general microwave switching networks. It is considered by many researchers as the most mature MEMS capacitive shunt switch available to date. For broadband application, the shunt configuration is preferred over a series configuration, because, in the up state, the coplanar wave guide (CPW) transmission line is continuous, resulting in fewer parasitic effects. In addition, in the down state, the isolation of the series switch is limited by the capacitive coupling between the two open conductors. An ultra broadband MEMS switch reported shows a highly reliable performance from DC to 110 GHz. The millimetre wave MEMS switch operates on low-voltage and can be realized on GaAs and Si [Chan *et al.*, 2003]. The switch is supported at its four corners by serpentine cantilevers. The device includes a metal bridge made entirely of gold that spans a CPW transmission line. In the up state, the switch is suspended approximately  $3 \mu\text{m}$  above the signal line. In the down state, the switch is pulled into direct metal-to-metal contact with the signal line creating a short circuit from the signal to the ground. A greater bandwidth and higher isolation are achieved using a  $\pi$ -design. The proposed switch consists of inductively resonant shunt switches in a  $\pi$ -network to achieve isolation at a lower frequency. The switch was developed by Peroulis *et al.* [Peroulis *et al.*, 2000] on a silicon substrate. The switch packet results in a 30dB isolation bandwidth of 10–20 GHz with an insertion loss of 0.2 dB and a return loss of 20 dB. This is an excellent performance expected from a capacitive shunt switch.

The MEMS series switch results in an open circuit in the t-line when no bias is applied (up-state position), and it results in a short circuit in the t-line when a bias voltage is applied (down state position). The switch is named a series switch because it is connected in series with the I/O port. Series switches are designed to operate from DC to higher frequencies, depending on the application. They use resistive or metal-to-metal contacts. Therefore they permit operation down to DC. The first Rockwell

Scientific series switch was developed by Yao and Chang and closely resembled the standard cantilever switch [Mihailovich *et al.*, 2001]. The switch is suspended 2–2.5  $\mu\text{m}$  above the substrate and the pull-down voltage is 60 V. Motorola recently developed a compact DC-contact MEMS series switch on silicon substrates. The HRL (formerly Hughes Research Laboratories) series MEMS switch was developed by Hyman *et al.* during 1998–2000 on GaAs substrates [Hyman *et al.*, 1999]. It is mechanically very similar to the first-generation Rockwell switch developed by Yao and Chang. The measured insertion loss is 0.1 to 0.15 dB over 1–40 GHz, indicating a total switch resistance of 1–1.5 ohm. The measured isolation is 45 dB at 4 GHz, and 25 dB at 40 GHz. McGruer and Zavracky at North-eastern University have teamed with Analog Devices to develop a very mature process for a DC-contact MEMS inline series switch on silicon substrates [Zavracky *et al.*, 1999]. The cantilever is suspended 0.6–1.2  $\mu\text{m}$  above the pull-down electrode, and it is fabricated using a thick layer of electroplated gold (7–9 m). The inline switch has a pull-down voltage of 60–80 V, with a switching time of 1–2  $\mu\text{s}$  (pull-down) and 2–3  $\mu\text{s}$  (release).

The present work in our research group is focussed on the design and development of a single-pole single-throw (SPST) and single pole double throw (SPDT) MEMS Switches for operation over a wide range of frequencies. Different types of RF MEMS series switches, shown in Fig.2, have been developed using the polyMUMPs foundry process [PolyMUMPs foundry handbook, V4].



**Figure 2. RF MEMS DC-contact switches fabricated using polyMUMPs process**

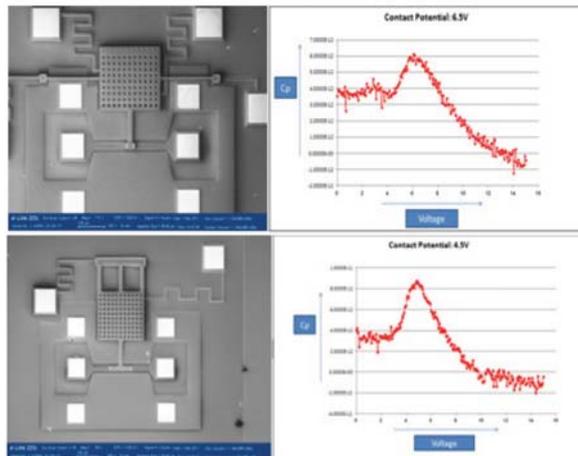
The polyMUMPs process starts with low resistivity silicon substrate. All electrical connections have been taken using the 0.5  $\mu\text{m}$ -thick Poly0

polysilicon layer. A 2.0  $\mu\text{m}$ -thick sacrificial oxide layer, Oxide1, has been utilized to create the air gap for electrostatic actuation. The actuation pad and output pad have been realized in the Poly0 layer. The beams are realized in a 2.0  $\mu\text{m}$ -thick Poly1 polysilicon layer. Standard pads of dimensions 100  $\mu\text{m} \times 100 \mu\text{m}$  have been imported from the polyMUMPs standard library. A dimple of height 0.75  $\mu\text{m}$  has been incorporated underneath the beams at their free end in order to reduce the beam end deflection to 1.25  $\mu\text{m}$ . The Anchor1 etch step has been utilized in order to fix one end of the beam to the base. In order to reduce while-release stiction, additional dimples at a regular distance of 100  $\mu\text{m}$  have been included underneath the beam. In order to reduce the torque generated on the beam by the electrical path connecting the bottom electrode to the pad, the electrical connections to the electrode have been spaced as closely to the anchors as possible. Fifteen samples of the devices have been fabricated. The size of each die is 1 cm  $\times$  1 cm and it consists of several other devices along with the switches. All the structures have been realized on top of a 0.6  $\mu\text{m}$ -thick silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer over the 675  $\mu\text{m}$ -thick  $\langle 100 \rangle$ -n-type silicon wafer. The low-pressure chemical vapour deposition (LPCVD) technique has been used to deposit the sacrificial layer oxides and the polysilicon layers. Reactive ion etching (RIE) has been utilized to create the anchors and the dimple. In order to release the structure, 49% hydrofluoric acid (HF) solution has been used to etch away sacrificial oxides. In order to increase the possibility of release and reduce while-release stiction, an additional critical point drying (CPD) step has been incorporated into the release process. All these steps are standardized in the polyMUMPs process. The final mask-layout for fabrication of the structures has been designed in the L-Edit Tanner tool.

The electromechanical behaviour of these switches has been studied through CV measurement using a DC probe station manufactured by Sus-Microtec, a DC voltage source and a LCR meter manufactured by Agilent. Some of the measured results are shown in Fig 3.

The polyMUMPs process contains poly-silicon as a structural layer, and is basically a three-layer process. Poly-silicon is a mechanically stable material with a Young's modulus of 160 GPa. It

improves the electromechanical performance of MEMS devices. After fabrication through the standard process, electrical, mechanical and RF performances of the devices have been experimentally investigated. Different kinds of MEMS switch membranes have been tested and characterized for mechanical and electrical responses.

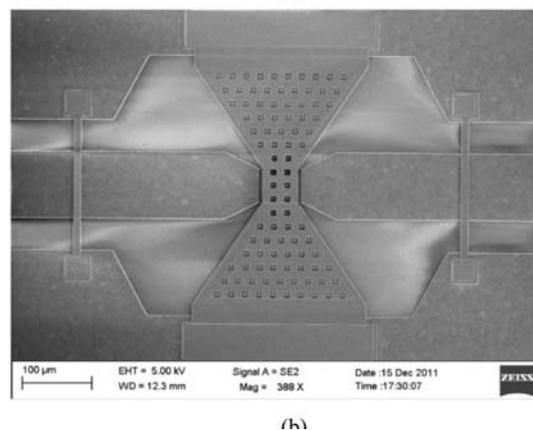
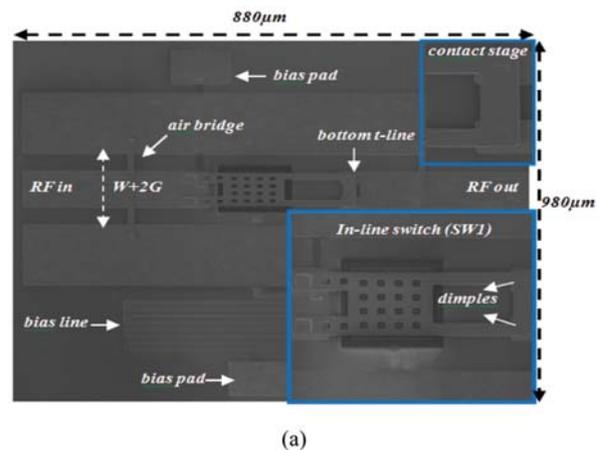


**Figure 3.** CV measurement analysis using a cantilever-based RF MEMS DC-contact switch

Electromechanical characterization gives an idea about the release process, although it contains both HF release and CO<sub>2</sub> dry release. A device-yield performance is also noticed through multiple testing. So, to understand the effect of release and electromechanical behaviors for different MEMS devices with various structural modifications, the polyMUMPs process plays a very important role in the first phase of the study. The process starts with a very low resistivity silicon substrate that is not suitable for RF applications, such as MEMS switches and phase shifters. Although polysilicon offers various advantages as per the MEMS process, it is not suitable material for RF and microwave application. To improve the RF performance, a custom-made process has been developed and switch design has been carried out with optimization for RF applications. Different configurations of an inline series switch, a single-pole double-throw switch, a high-isolation switch and a capacitive shunt switch have been developed using this RF-compatible process. The mechanical, electrical and RF response of these devices have been experimentally investigated.

## 2.1 RF-compatible Process

The process starts with a 0.025" thick alumina substrate polished on both sides. The relative permittivity of the substrate is 9.8 with a loss tangent of 0.0001 at 1 MHz. Alumina substrate is used in this work because of its good mechanical strength, good electric insulation and high temperature-stability.



**Figure 4.** SEM image of fabricated RF MEMS switches (a) MEMS DC-contact series switch (b) MEMS shunt switch.

After the RCA cleaning of the wafer, the first resistive layer of titanium tungsten (TiW) is deposited and patterned using the lift-off technique. This layer is used to electrically bias the circuit by mask 1. The sheet resistance of this layer is 20 Ω/sq. A 0.7 µm-thick SiO<sub>2</sub> layer is deposited at 250°C by plasma-enhanced chemical vapour deposition (PECVD) and patterned using reactive ion etching (RIE). RIE is employed to pattern the oxide and remove the patterning photoresist (PR). This is a passivation layer and deposited on the last layer (TiW) by mask 2. An SEM image of the MEMS

series and shunt switches fabricated are shown in Fig. 4.

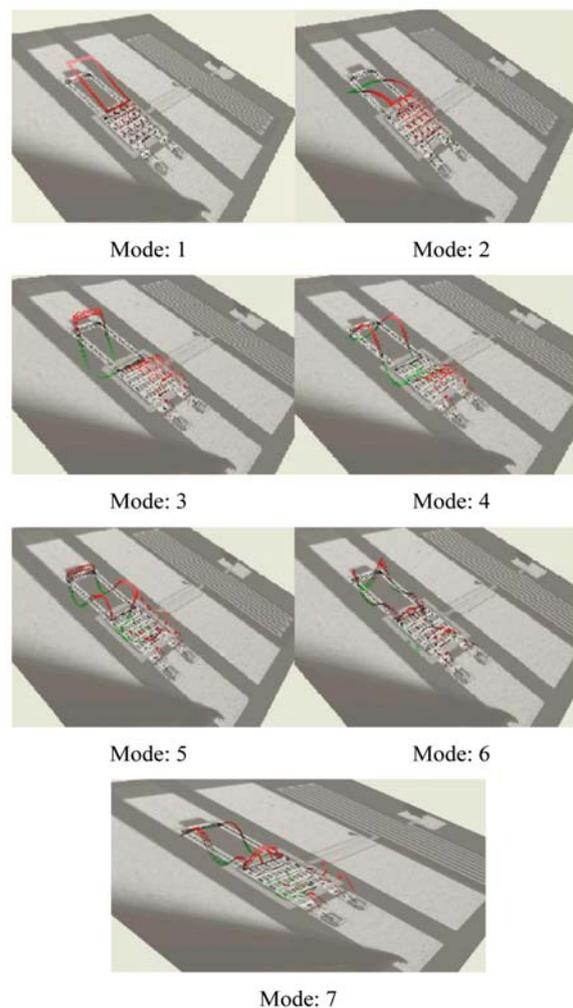
An evaporated 400 Å chromium/70 nm gold bi-layer is deposited as a seed layer. A photo-resist mould is formed in the third lithographic step and 2 μm gold is electroplated inside the mould. The mould and seed layers are to be removed afterwards. Chromium is applied as an adhesion layer for the gold. This layer is used to pattern the CPW line, fixed electrodes and bias pad by mask 3. A 300 Å TiW film is sputtered followed by the deposition of 0.5 μm silicon oxide using PECVD at 250°C. The dielectric and TiW layers are dry etched in RIE in order to pattern them using a mask layer. The TiW layer serves as an adhesion layer binding silicon oxide to gold. This layer is patterned by mask 4 to make an insulation layer on a CPW line and on electrodes. Spin-coated polyimide (PI) is used as the sacrificial layer for this process. Initially, it is coated to a thickness of 2.5 μm. Next, it is patterned by mask 5 (anchor mask) in an RIE step to etch the PI and fully clear the anchor holes. Furthermore, dimple openings are made in polyimide using an RIE etching step using the pattern of mask 6. The depth of etching is set to be 1 μm. The top gold layer consists of a sputtered gold seed layer plus electroplated gold. The total thickness of this layer is 2 μm, and it is used as the structural layer for the devices. The negative PR moulding method is used to define this layer. This layer is patterned to make a mobile electrode by mask 6. The sheet resistance of this layer is 0.02 Ω/sq. The last step is the release process. In this process, the sacrificial layer is removed by RIE in an oxygen plasma.

## 2.2 Experimental Analysis of MEMS Switch

MEMS switches are core components for implementing switched-line MEMS phase shifters. Metal-to-Metal contact cantilever series in-line switches are employed due to their good performance and compact size. Electromechanical behavior analysis with parametric optimization of a MEMS switch has been carried out using the Coventor-ware 2010, Saber platform. The mechanical response, electrical response, transient analysis, intermodulation distortion (IMD) and the RF response of MEMS switches have been experimentally investigated and validated using system level simulation and are presented in the subsequent section.

### 2.2.1 Mechanical response

The voltage actuation method has been used to detect mechanical vibrations of the MEMS switch. A small signal frequency sweep has been imposed over a dc actuation voltage to observe the frequency response of a particular structure. The out-of-plane vibration amplitude response has been recorded for the frequencies of the signal. A Polytec-made Laser Doppler Vibrometer (LDV) has been used to detect the displacement of the structure in the out-of-plane direction. The LDV uses the Doppler frequency shift method to calculate the displacement due to external excitation at the point where the laser pointer is focused. Seven modes of vibration have been captured from LDV up to 0.5 MHz frequency and these are shown in Fig.5. The vibration spectrum of the MEMS switch with applied external excitation is shown in Fig.6.



**Figure 5** Various modes of vibration of a MEMS switch up to 0.5 MHz.

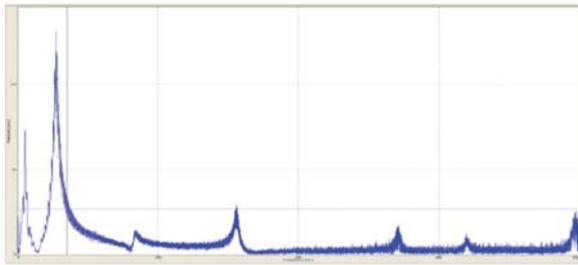


Figure 6 Vibration spectrum of MEMS switch

### 2.2.2 Electrical response

The electrical characterization of the push-pull bridge has been carried out using an Agilent 4284A LCR meter with a probe station. To measure the  $C$ - $V$  characteristics of MEMS switches, the bottom fixed electrodes have been grounded and the required voltage sweep from 0 to 35V has been applied to the top suspended cantilever beam using the probes. A small ac signal of 5 MHz has been imposed on the dc actuation voltage to measure the capacitance. Open circuit offset measurement corrections were made before recording the capacitance values.

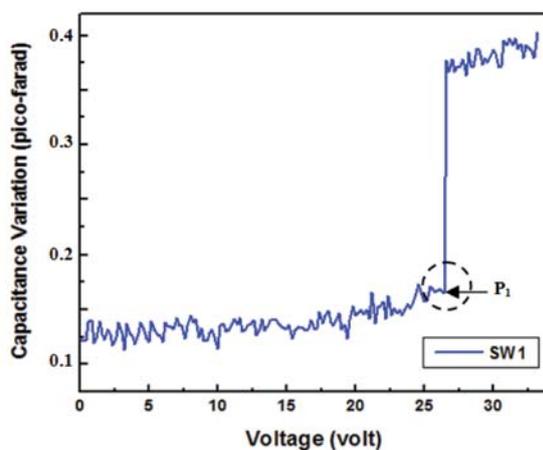


Figure 7. Capacitance versus voltage measurement of MEMS switch shows pull-in at 26 volt

The measured point of instability of the switch occurs at point  $P_1$  with an actuation voltage of 26 V, above which the bridge suddenly snaps, down with an abrupt change in capacitance value, as shown in Fig. 7.

### 2.2.3 Switching time analysis

Switching time is a critical specification of MEMS switch dynamics. These switches are based

on mechanical movement between the open and closed states, and the actuation speed is limited by the mechanical response time. The actuation dynamics is nonlinear and numerical modelling has been used to characterize the switch dynamics.

Switching time measurement has been carried out using the Agilent infiniium DSO-X 92504 25 GHz high frequency digital storage oscilloscope. A square wave of 0 to 40 V at 1 kHz was imposed on the actuation pad of the switch and the corresponding effects on switching and release time recorded on the Agilent Digital Storage Oscilloscope (DSO). In this work, switch actuation voltage has been considered to be 1.5 times the pull-in voltage.

The measured switching time and release time of MEMS DC-contact switch are 89  $\mu$ sec and 143  $\mu$ sec respectively, as shown in Fig 8.

### 2.2.4 Loss analysis

The cantilever DC contact MEMS switch is the key element in the switched-line phase shifter. It has been noticed that the fabricated DC contact MEMS switches do not suffer from stiction and dielectric charging problems, when operated un-packaged.

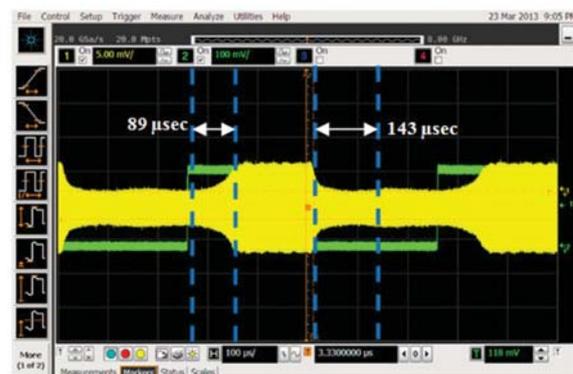


Figure 8 Measurement of switch ON(89msec) and OFF(143msec) time.

When the membrane is at the up position, it exhibits a very small capacitance which will block the RF path. When the actuation voltage is applied between the membrane and the bottom electrode, the membrane will be pulled down and it will be in DC contact with the bottom t-line that connects to the output transmission line ( $RF$  out) as shown in Fig 4(a). The MEMS switch in the ON-state has a very small contact

resistance and provides a through path to the RF signal.

The equivalent circuit model of a DC contact MEMS switch in the ON- and OFF-states is shown in Fig.9. As shown in Fig 9(a), when the DC contact MEMS switch is in the OFF-state (the membrane at the up position), it is modeled as a small inductance ( $L$ ) of 115 pH in series with a small resistance ( $R_t$ ) of 0.6  $\Omega$  and a small capacitance ( $C_{off}$ ) of 11.13 fF and in parallel connection with a small capacitance ( $C_p$ ) of 27 fF. The capacitance  $C_{off}$  is from the parallel plate between the membrane and the bottom contact metal connecting to the output transmission line, while the parallel capacitance  $C_p$  is from the parallel plate between the membrane and the bottom fixed electrode. The 0.5  $\Omega$  resistance ( $R_t$ ) is used to model the transmission line loss. The  $L_s$  and  $C_s$  are the t-line inductance and capacitance which offer 50  $\Omega$  to the RF input and output transmission lines.

When an actuation voltage is applied between the membrane and the bottom electrode, the switch will be activated and in the ON-state, its membrane will be pulled down and is in DC contact with the bottom t-line. The switch will thus exhibit a contact resistance ( $R_{ON}$ ) which is extracted to be around 3.7  $\Omega$  from the measurements. The equivalent circuit model is shown in Fig. 9(b). As can be seen, when the DC contact MEMS switch is in the ON-state, it is modeled as a small inductance (115 pH) in series with a resistance  $R_{ON}$  and in parallel with a capacitance ( $C_{pon}$ ) of around 37 fF. The inductance ( $L$ ) of 115 pH remains the same even when the MEMS switch is in the ON-state. The  $C_g$  ( $\approx 6 - 8$  fF) refers to the signal-line coupling capacitance due to the gap between each broken signal line. Since the membrane is in DC contact with the bottom output transmission line in the ON-state, the series capacitance ( $C_{off}$ ) is removed, the switch shows a slightly higher resistance than the equivalent circuit model in the OFF-state (Fig. 9(a)). This resistance is partially from the small transmission line loss (0.6  $\Omega$  in Fig 9(a)), and partially from the MEMS contact resistance ( $R_c$ ). As also noted in Fig. 9(b), the capacitance ( $C_{pon}$ ) in parallel is larger than the parallel capacitance ( $C_p$ ) in Fig 9(a) when the switch is in the OFF-state.

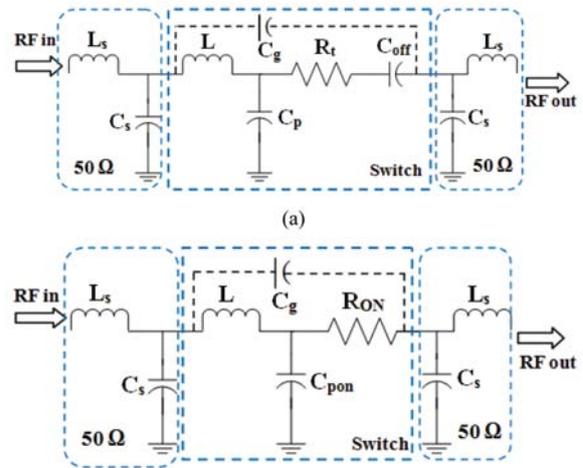


Figure 9 Equivalent circuit model of switch in (a) OFF and (b) ON state.

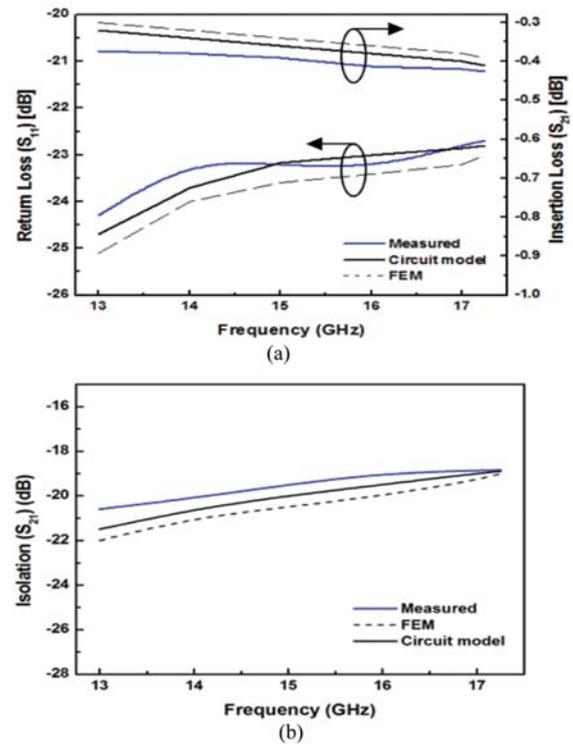


Figure 10 Measured S-parameters of RF MEMS switch versus circuit model and FEM based simulation results (a) Return loss and insertion loss (b) Isolation

The RF measurements on the switch have been performed using an Agilent 8510C vector network analyzer with GSG RF probes, and a Cascade DC probe. The SOLT method was used for calibration. A measured actuation voltage of 26 V was used to characterize the MEMS switch. The measured RF responses of the switch in the ON-

and OFF-states are shown in Fig 10, against finite element method (FEM)-based HFSS and circuit model-based ADS simulations. Switch SW1 gives isolation better than 17.5 dB, a worstcase insertion loss of 0.427 dB and a return loss better than 22.7 dB in the frequency band 13 – 17.25 GHz. The measured results have been successfully validated using simulation results within a 6% tolerance limit, the deviation being mostly due to signal leakage via the TiW bias lines.

### 2.2.5 IMD analysis of MEMS switch

The inter modulation distortion (IMD) of the DC-contact MEMS switch has been examined in this work. The third-order-intercept-point (IIP3) has been experimentally determined using two signal generators with carrier frequencies  $f_1=16.999998$  GHz and  $f_2=17.000013$  GHz, respectively, with a spacing of 3kHz, which is much less than the switch mechanical resonance frequency (9 kHz). A power combiner is used in the measurement, which has a loss of -12 dBm (including cable loss at 17 GHz). Two-tone IMD has been performed on SW1 and SW2 where  $2f_2 - f_1 = 17.0000053$  GHz and  $2f_1 - f_2 = 16.9999947$  GHz.

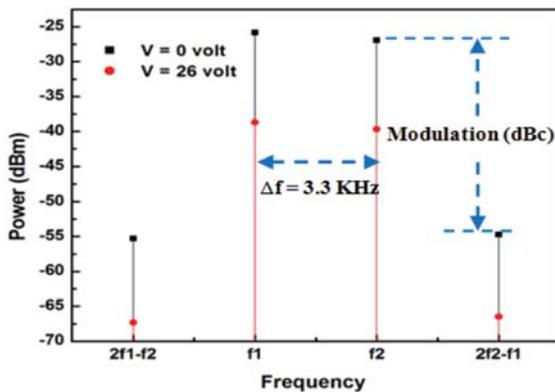


Figure 11 shows the IIP3 measurements of the switch. Linearity has been observed up to 18 dBm of input power. The measured IIP3 of switch is 6.4 dBm which shows that the switch offers good linearity within operating frequency range.

### 2.2.6 MEMS shunt switch

The RF MEMS shunt switch consists of a metal bridge (MEMS bridge) suspended over the coplanar waveguide (CPW), a dielectric layer coated on the signal line as shown in Fig.12. The biasing circuitry is not shown in the figure. The switching operation of the switch is achieved by

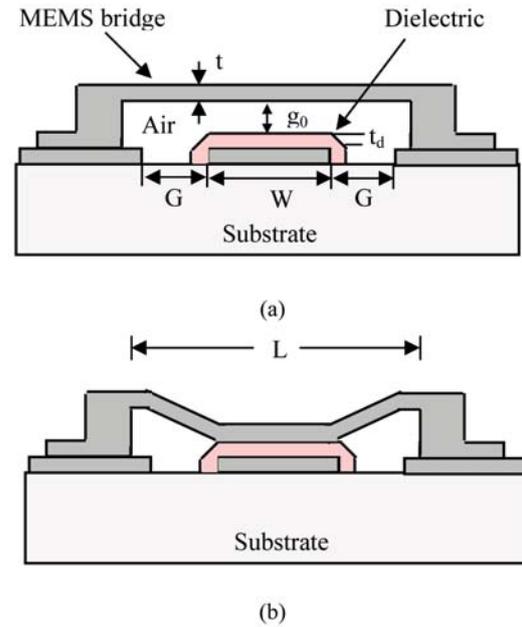


Figure 12 Schematic showing a MEMS capacitive shunt switch in (a) ON-state, (b) OFF-state.

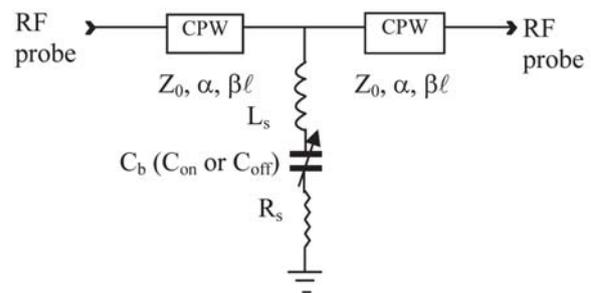


Figure.13 Equivalent CLR model of a MEMS capacitive shunt switch.

When un-actuated, the air dielectric between the two electrodes exhibits a very low capacitance, given by:

$$C_{on} = C_{pp} + C_f \quad (1)$$

where  $C_f$  is the fringing capacitance and  $C_{pp}$  is the parallel plate capacitance which is expressed as

$$C_{pp} = \left( \frac{t_d}{\epsilon_d + A} + \frac{g_0}{\epsilon_0 A} \right)^{-1} \quad (2)$$

$\epsilon_d$  and  $\epsilon_0$  are the relative permittivity of the dielectric layer and air, respectively,  $t_d$  is the thickness of the dielectric layer and  $g_0$  is the air-gap between the bridge and the dielectric layer when the switch is in the up-position.  $A$  is the

overlapping area between the bridge and the bottom signal line. For typical switch dimensions, the ON-state capacitance is of the order of femto farads.

Unlike parallel plate capacitance, there are no design equations for the fringing capacitance. This leads to the use of 3-D electrostatic simulators in calculating it, as done in [Muldavin *et al.*, 2000]. Though the effect of fringing field in electromagnetic parallel-plate actuators is a well-understood phenomenon, the existing formulations often result in complicated mathematical models from which it is difficult to determine  $C_f$ . Therefore, in this work, curve-fitted closed form expressions were derived to calculate the ON-state capacitance and series inductance of the switch. The proposed expressions are valid only for the case of the flat-bridge profile but can be used for buckled membrane as well, provided that the air-gap height is accurately measured. The proposed expression to calculate the ON-state capacitance of the switch is given as

$$C_{on} = \begin{cases} (A) \times (B)^{0.75} \times (g_0 C)^{0.05}; & g_0 < 2 \\ A & ; \quad g_0 = 2 \\ (A) \times (B) \times (C)^{0.24} & ; \quad g_0 > 2 \end{cases} \quad (3)$$

where,

$$A = (0.6w)^{0.98} \quad (4)$$

$$B = \left( \frac{2}{g_0} \right) \quad (5)$$

$$C = \left( \frac{W}{w} \right) \quad (6)$$

Here,  $w$  is the width of the bridge,  $g_0$  is the gap between the bridge and the dielectric layer.

The series inductance  $L_s$ , OFF-state capacitance  $C_{off}$ , and the series resistance  $R_s$  are important parameters of the switch in the down (OFF)-state. The down-state parameters of the switch are relatively easy to calculate using simple equations. For instance,  $C_{off}$  is a capacitance of a simple metal-insulator-metal (MIM) capacitor formed by the top electrode (bridge) and lower electrode (signal line of the CPW) with a thin dielectric layer sandwiched between the two metal electrodes and is given by

$$C_{off} = \frac{\epsilon_0 \epsilon_d A}{t_d} \quad (7)$$

In the RF perspective,  $C_{off}$  controls the response of the switch for  $f < f_0$  [Muldavin *et al.*, 2000]. Due to uniqueness of this characteristic of  $C_{off}$ , its value can be accurately extracted by curve-fitting the measured isolation results of the switch with the equivalent circuit for  $f < f_0$ .

Once  $C_{off}$  is known,  $L_s$  determines the resonant frequency of the switch and is obtained by (8).

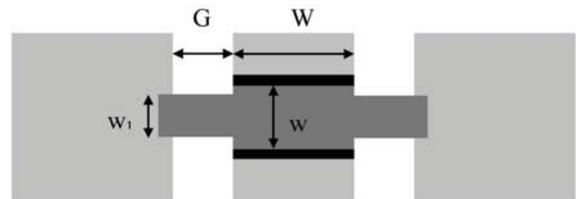
$$f_0 = \frac{1}{2\pi\sqrt{L_s C_{off}}} \quad (8)$$

Here,  $f_0$  is the series resonant frequency of the switch. It is apparent that the exact value of inductance  $L_s$  depends upon accurate extraction of  $C_{off}$  obtained by curve-fitting. However, in most of the cases, the bridge doesn't form an intimate contact with the lower electrode due to fabrication-induced failure modes such as buckling of bridge and surface roughness [Yu *et al.*, 2005]. This limits  $C_{off}$  to a value between 30-50 % of the actual designed value.

In order to calculate  $L_s$  directly using the dimensions of the MEMS bridge, we have evolved a closed form expression using curve-fitting techniques. The inductance of a switch having a bridge with rectangular cross-section is expressed as

$$L(pH) = (G \times w^{-(0.003 \times G)}) - 19.887 \quad (9)$$

where  $G$  is the width of the CPW slots and  $w$  is the bridge-width. The expression for inductance of the switch can also be used for the inductive step-in-width bridge geometry such as shown in Fig.14. However, in that case,  $w$  should be replaced by  $w_1$ .

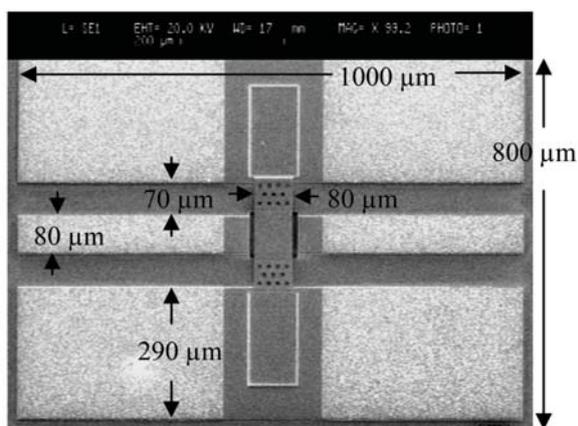


**Figure 14 Schematic showing step-in-width bridge-profile.**

The circuit modeling of the switch is done using ADS. S-parameters measurements were performed using an Agilent E83638 vector network

analyzer and a Cascade Summit 12651B-6 RF probe station. Prior to testing, on-wafer calibration is done over the 0.5-26.5 GHz frequency range using LRM standards. The DC voltage required to actuate the MEMS capacitors was fed to the bias network from a dual output DC power supply (Agilent E3620A).

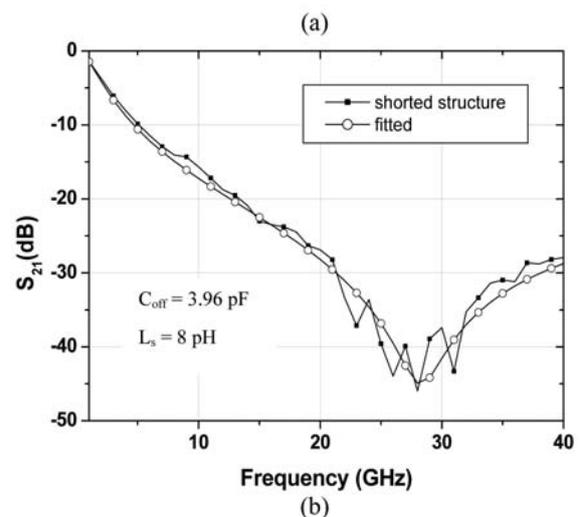
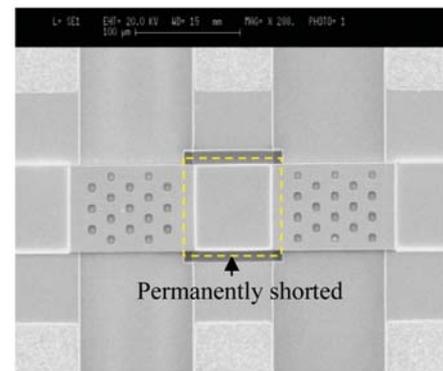
The switch is fabricated on a 500- $\mu\text{m}$  GaAs ( $\epsilon_r=12.9$ ) substrate and is shown in Fig. 15. The thickness and permittivity of the dielectric layer are 0.1  $\mu\text{m}$  and 7, respectively. The fabricated test structure is a replica of the switch in which the bridge is permanently shorted with CPW center conductor through dielectric layer, as shown in Fig. 16(a). Since the test switch is free from failure mechanisms commonly seen in MEMS switches in down-state, it serves as an ideal structure to validate our proposed expression for  $L_s$ .



**Figure 15** Fabricated switch on 500- $\mu\text{m}$  thick GaAs wafer

The measured isolation of the test structure and its equivalent switch parameters are shown in Fig. 16(b). The switch parameters are obtained by curve-fitting the measured result with the CLR model. Based on the extracted data, the expression is found to be in complete agreement with the measured results and the inductance is measured as 8 pH, as shown in Fig. 16(b).

Results obtained from the validation reveal that the proposed expressions for ON-state capacitance and series inductance are quite satisfactory and give accurate results for a typical range of MEMS switch dimensions.



**Figure 16** MEMS test switch (a) SEM image (b) Measured and fitted results of the MEMS shunt switch

### 2.2.7 MEMS high-isolation switch

Several methods are reported in the literature for the design of high-isolation switches. Metal-contact series MEMS relays [Lee *et al.*, 2004, Mihailovich *et al.*, 2001], using composite bridge structures with the smaller contact areas and a much broader signal line gap, achieve a good isolation from DC to 40 GHz, but the process is relatively complex and the isolation cannot reach up to 40 dB in the X/Ku band. If the isolation characteristics of switches are lower, then higher intermodulation results due to leakage of signals from another channel. This will result in deterioration of RF system performance [Lee *et al.*, 2004]. Series-shunt configuration that is commonly used to improve the isolation in wideband PIN-diodes or FET switches can also be realized using integrated MEMS technology [Zhu *et al.*, 2004]. Examples are the absorptive MEMS switches [Tan *et al.*, 2001], capacitive series-shunt switches [Muldivin *et al.*, 2006] and DC-contact series-shunt switches

[Santors *et al.*, 2005, Renes *et al.*, 2005]. Capacitive shunt MEMS switches result in high isolation using inductive tuning or multi-bridge tuning at X/Ku/Ka band, but it is not suitable for wide band applications. For increasing the isolation, one series and two shunt switch structures are used; the shunt switches are separated by a quarter-wavelength section of a transmission line. The proposed series-shunt switch configuration is ideally suited for applications up to 12 GHz (X-band).

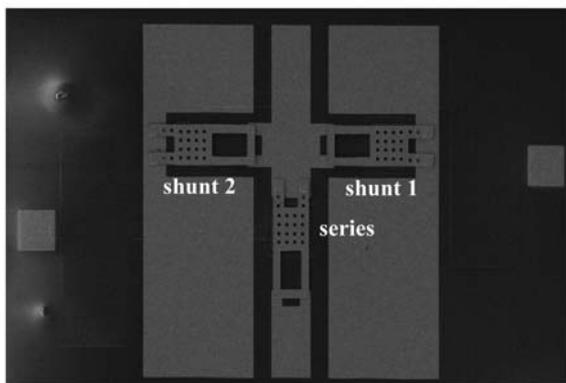


Figure 17 Micro-fabricated image of high isolation switch

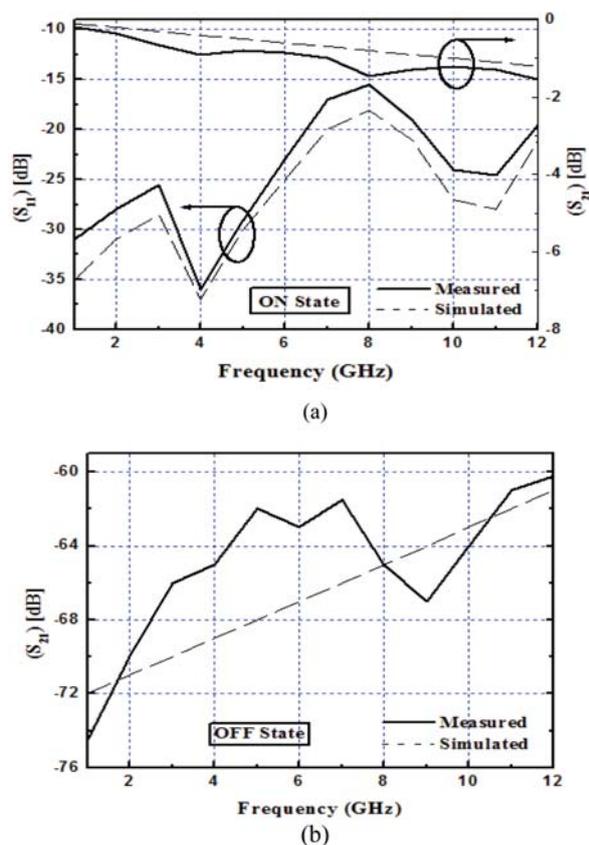


Figure 18 Measured S-parameter of high isolation switch (a) ON-state (b) OFF-state Isolation up to 12 GHz

In this study, we have focused on the development and characterization of compact series-shunt switches with high-isolation characteristics. To avoid the fabrication complexity and biasing problem, three identical metal-contact MEMS switches are employed. The same, gold-based surface micromachining process is used to develop high-isolation switch. An SEM image of the switch is shown in Fig. 17.

From Fig.18, it is observed that a return loss of better than 15 dB and a worst-case insertion loss of 1.58 dB has been obtained for the ON-state condition. Furthermore, isolation better than 60 dB has been achieved in the OFF-state condition up to 12 GHz, as shown in Fig 18(b).

### 2.2.8 MEMS SPDT switch

Single-Pole Double-Throw switches are more sophisticated than the previous one. In this case, there is one input and two outputs and it requires coordination between the different elements so as to route the signal to the correct port. In fact, the most complex part of the design is to decide the structure that will be used. An important part of the design is the distance between the MEMS switches and the reactive junction for different series and shunt switches. The input reflection co-efficient can be improved by the addition of a short high-impedance section before the reactive junction. The SPDT switch is one of the key components used in transmit/ receive modules, as illustrated in Fig. 19.

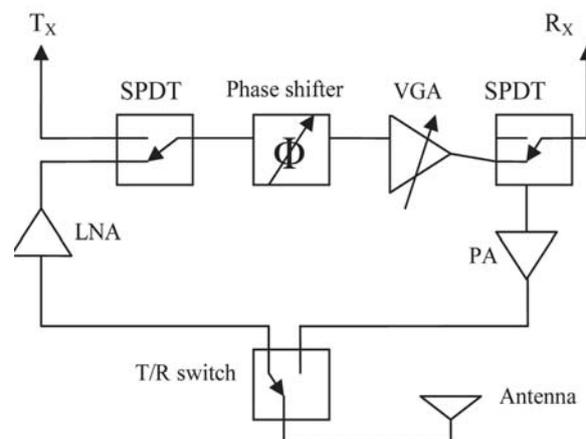


Figure 19 Schematic of the T/R module, where three SPDT switches are used.

Many research groups have reported research results on improving isolation in the SPDT switch for certain specific frequency bands of interest. SPDT switches have been developed using a capacitive shunt-type switch or a DC-contact switch [Pacheco *et al.*, 2001, Yamane *et al.*, 2011, Cho *et al.*, 2010]. These types of MEMS switches utilize electrostatic actuation to change the signal path and generally require two independent voltages to switch between the two ports. In our work, the SPDT switch has been developed using two high isolation-based series-shunt SPST switches.

Measured return loss of better than 22 dB, worst-case insertion loss of 1.45 dB and isolation better than 45 dB have been obtained from the SPDT switch in the Ku-band. Measured port-to-port isolation is 29 dB. The present state-of-the-art of the SPDT switch in the Ku-band is tabulated in Table-I.

**Table1: state-of-the-art of rf mems spdt switches**

Functional Parameter	SPDT switch performance			
	[31]	[32]	[33]	Our work
Frequency (GHz)	20	12	20	17
Bias voltage (volt)	9	85	4.3	40
Switching time ( $\mu$ sec)	NA	40	132	78
Loss (dB)	0.95	0.56	2.05	1.45
Matching (dB)	NA	19.4	NA	22
Isolation (dB)	40	51.4	36	45
Area ( $\text{mm}^2$ )	4.4	5.25	NA	1.25

We have implemented a miniaturized high-isolation MEMS SPDT switch up to Ku-band. Mechanical, electrical and RF response of a single-MEMS switch has been experimentally investigated and presented. Return loss of better than 22 dB and insertion loss of 1.45 dB have been obtained with 40 V actuation and 78  $\mu$ s switching time from the fabricated SPDT switch. The isolation has been measured as 45 dB up to 17 GHz. To reduce the insertion loss further in the entire operating frequency range, CPW and bias lines should be optimized to prevent signal leakage.

### 3. RF Varactor

Micro-electromechanical Systems (MEMS) technology is primarily used to develop miniaturized,

integratable, high-quality factor (Q), frequency-selective circuits. High-Q devices are fundamental for different passive and active circuits and can substantially reduce the phase noise or power consumption of oscillators and amplifiers [Rebeiz., 2003]. The Voltage-Controlled Oscillator (VCO) at RF frequency is composed of a CMOS circuit and an LC tank in the conventional negative- $g_m$  topology. So, the capacitance change in the MOS capacitor limits the tuning range and the operating frequency of the VCOs and the nonlinearity of the tuning devices degrades the phase noise of the RF VCOs [Dec *et al.*, 2000]. Tunable MEMS capacitors have been shown to give an adequate quality factor when they are fabricated using either aluminium or silicon or gold surface micromachining technology. These devices are expected to offer an excellent linearity since they do not respond to high frequencies outside their mechanical resonance frequencies [Dec *et al.*, 1998]. The tunability of the VCOs depends on the tuning range of the capacitors in the tank circuits. Lesson's formula of phase noise of a VCO describes the inverse square relationship between phase noise and Q- factor of the tank circuit [Dec *et al.*, 1998]. From that, it is evident that phase noise performance can be improved by increasing the Q-factor of the tank circuit. Since on-chip inductors do not possess very high Q values, the Q-factor of the varactor device needs to be increased. On-chip MOS varactors are very difficult to realize with a low phase noise and a high quality factor that can sustain wide process and temperature variation [Nieminen *et al.*, 2004]. The MEMS-based varactor is therefore a good replacement for on-chip MOS varactors in this regard. Due to low loss, the MEMS varactor possesses the property of very high Q values and is capable of withstanding wide process and temperature variation. In addition, conventional micro-machined tunable capacitors [Michael *et al.*, 1998] are not expected to respond to RF frequencies in the 1–2 GHz range, especially since their mechanical resonant frequencies normally lie in the 10–100 kHz range. Therefore, with RF frequencies 10,000 times the mechanical bandwidth, these devices are unlikely to produce a significant amount of harmonic content [Mahony *et al.*, 2003]. The main limitation of these devices, however, has been that their tuning ranges thus far have been less than the theoretical calculations

suggested [Fedder *et al.*, 2005]. In this paper, design optimization and simulation of two parallel-plate variable capacitor for VCO applications, using the method of electrostatic actuation, is presented. Suspension beams have been optimized for 3.3 V VCO power supply. The working principle is derived from changing the gap between two parallel plates using electrostatic actuation, one is fixed on the substrate and the other is suspended with four T-shaped suspension beams.

### 3.1 Varactor design

Electromechanically tunable capacitor consists of two parallel plates, four T-shaped suspension beams to suspend the top plate as shown in Fig.20. The top plate is pulled down to bottom plate with electrostatic force.

The dynamics of an electromechanical two plate varactor can be expressed using (10) [Rebeiz, 2003]

$$m \frac{d^2 x(t)}{dt^2} + b \frac{dx(t)}{dt} + kx(t) = \frac{1}{2} \frac{dc_d(t)}{dx} V_1^2(t) \quad (10)$$

where  $m$  is the mass of the suspended plate,  $b$  is the mechanical resistance,  $K$  is the effective spring constant,  $C_d$  is the desired capacitance and  $V_1$  is the applied electrostatic potential between two parallel plates. The current flowing through the desired capacitance is given by (11) [Rebeiz, 2003]

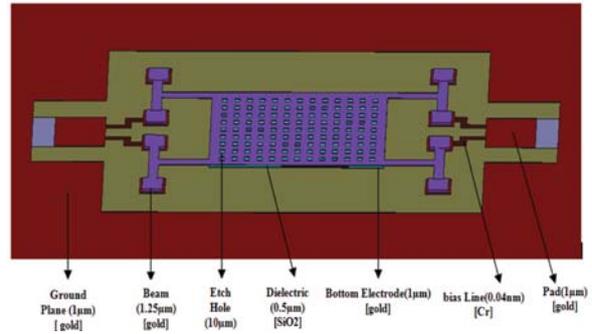
$$i(t) = C_d(t) \frac{dv_1(t)}{dt} + V_1(t) \frac{dC_d(t)}{dt} \quad (11)$$

The suspended plate moves towards the fixed plate until a point of instability occur where electrostatic force become exactly equal to the spring restoring force, corresponding to a 50% capacitance increase. The equilibrium between the forces can be mathematically represented as given by (12).

$$kx = \frac{1}{2} \frac{dc_d}{dx} V_1^2 = -\frac{1}{2} \frac{\epsilon_d A V_1^2}{(d_1 - x)^2} \quad (12)$$

where  $x$  is the displacement under dc condition,  $\epsilon_d$  is the dielectric constant of the medium ( $\epsilon_d = \epsilon_{air} \epsilon_0$ , where  $\epsilon_{air} = 1.00054$  and  $\epsilon_0 = 8.854 \times 10^{-12}$  F/m),  $A$  is the overlapping area of two parallel plates, and  $d_1$  is the separation of the capacitor plates when spring is in its relaxed state.

$$\text{Tuning Ratio (TR)} = \frac{C_{\max}}{C_{\min}} = \frac{\epsilon A / (2x/3)}{\epsilon A / x} = 1.5 \quad (13)$$



**Figure 20: Schematic illustration of variable capacitor on substrate**

In theory, the suspended plate can be pulled down at most by 1/3 of the original gap, so the maximum capacitance that can be tuned is  $\frac{3C_d}{2}$ , and maximum theoretical tuning range would be 1.5:1 as shown in (13)

Incorporating a worst-case-scenario fringing capacitance ( $C_f$ ) of 40% of  $C_{\max}$  as indicated in [Dec *et al.*, 2000, Dec *et al.*, 1998, Dec *et al.*, 1998, Nieminen *et al.*, 2004, Michael *et al.*, 1998], the value of capacitance tuning ratio obtained is given by (14)

$$\text{TR} = \frac{C_{\max} + 0.4C_{\max}}{C_{\min} + 0.4C_{\max}}, \text{ since } C_{\max} = 1.5C_{\min} \quad (14)$$

A semi-analytical model of the pull-in voltage can be obtained from [Mahony *et al.*, 2003]. It is based on calculation of the total potential energy content of a fixed-fixed beam subject to electrostatic actuation without considering the fringing field effects, and then a correction factor is applied to account for the fringing field effects. The first-order fringing field effects have been approximately compensated by an effective beam width. The following the pull-in voltage can be obtained, as given by (15), [Mahony *et al.*, 2003].

$$V_{PI} = \sqrt{\frac{1}{\left(1 + 0.65 \frac{x}{w}\right)}} \times \sqrt{\frac{c_1 E h^3 x^3}{\epsilon_0 l^4} + \frac{c_2 (1-\nu) x_0 h \sigma_0}{\epsilon_0 l^2}} \quad (15)$$

The constants  $c_1 = 11.7$  and  $c_2 = 3.6$ ,  $E$  is the Young's modulus and  $\nu$  is the Poisson's ratio,  $x$  is the gap between the two parallel plate,  $l$  and  $h$  are

the beam length and width respectively,  $w$  is the thickness of the beam and  $\epsilon_0$  is the permittivity of free space.

$C_0$  is the original capacitance without applying voltage or RF signal,  $K_m$  the effective spring constant of the four T-shaped beams, which can be written as (16).

$$K_m = 4K_{eq}, K_{eq} = \frac{k_1 2k_2}{k_1 + 2k_2}, k_i = \frac{Ew_i T_i^3}{L_i^3} \quad (16)$$

$K_{eq}$  is the equivalent spring constant of each T-shaped beams,  $L_i$ ,  $W_i$  and  $T_i$  are the length, width and thickness of the beams and  $E$  is the Young's modulus of the material.

Various sources of loss can affect the quality factor at high frequency. In our design, the two-plate varactor is modeled with conductive and resistive plates. This is justified in our case where the top plate is deposited with gold and the bottom plate is made of gold coated with silicon-dioxide.

The expression of the quality factor of varactor can be obtained from the input admittance of the varactor and is given by (17) [Fedder *et al.*, 2005]

$$\frac{Q+1}{Q-1} = \frac{\sin(\sqrt{2\omega\tau}) + 2\cos\left(\sqrt{\frac{\omega\tau}{2}}\right)\sin\left(\sqrt{\frac{\omega\tau}{2}}\right)}{\sinh(\sqrt{2\omega\tau}) + 2\sinh\left(\sqrt{\frac{\omega\tau}{2}}\right)\cos\left(\sqrt{\frac{\omega\tau}{2}}\right)} \quad (17)$$

where  $\tau$  is the time constant of the varactor that is given by (18)

$$\tau = R_p C_D \quad (18)$$

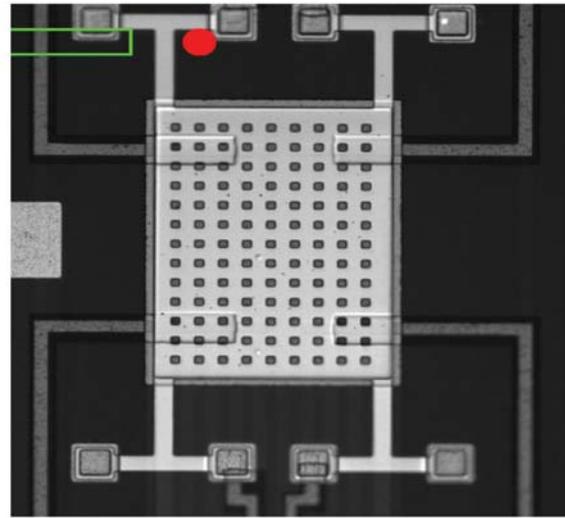
Here,  $R_p$  is the resistance of the resistive plate (i.e., sheet resistance for a square plate capacitor) and  $C_D$  is the total capacitance between the two parallel plates and  $w$  is the operating frequency in radian.

Since losses due to interconnect and the substrate parasitic are not considered in our design, the expression presented above represents the maximum theoretically achievable Q-factor. More detail parametric optimization of the reported varactor can be found in [Dey *et al.*, 2012]

An image of the micro-fabricated MEMS varactor is shown in Fig. 21. Material properties are listed in Table II.

**Table 2: Material Properties of fabricated mems varactors**

No	Material Properties	
1	Young Modulus of gold	45 GPa
2	Conductivity of gold	$4.1 \times 10^7$ S/m
3	Sheet resistance of bottom gold electrode	0.025 $\Omega$ /square
4	Sheet resistance of top gold electrode	0.02 $\Omega$ /square
5	Poisson ratio of gold	0.4
6	Density of gold	19300 kg/m <sup>3</sup>



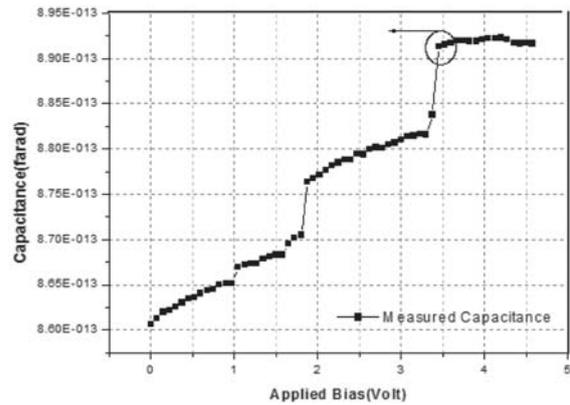
**Figure 21 Micro-fabricated image of MEMS varactor**

Mechanical and electrical tests have been performed on the varactors to examine the characteristics of the structure. Voltage actuation method has been used to detect the mechanical vibrations of the varactor. Small signal frequency sweep has been imposed over a dc actuation voltage to observe the frequency response of the particular structure. The out-of-plane vibration amplitude response has been recorded for the frequencies of the signal. A Polytec-made Laser Doppler Vibrometer (LDV) has been used to detect the displacement of the structure in the out-of-plane direction. The LDV uses the Doppler frequency shift method to calculate the displacement due to external excitation at the point where the laser pointer is focused. The vibration spectrum of the MEMS varactor with applied external excitation is shown in Fig. 22(a). The first mode of vibration of

the structure at 1.475 kHz which is obtained from LDV is given in Fig. 22(b).

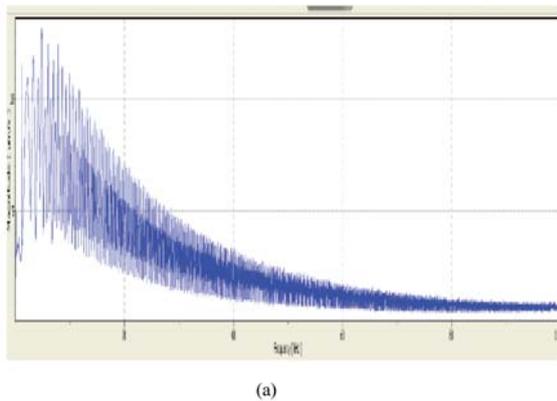
The variation of capacitance with actuation voltage of the structure has been measured using a DC probe station manufactured by Sus-Microtec, a DC voltage source, and a LCR meter manufactured by Agilent.

To measure the C-V characteristics, the bottom fixed plate of the varactor is grounded and the required voltage sweep from 0 V to 2.5 V is applied to the top suspended electrode using the probes. A small AC signal of 5 MHz is been imposed on the DC actuation voltage to measure the capacitance. Open circuit offset measurement corrections were made before recording the capacitance values. The capacitance of the varactor with change in voltage has been observed and plotted by the LCR meter as shown in Fig. 23.

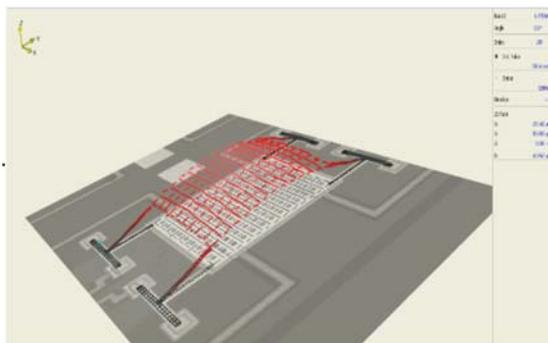


**Figure 23 Measured capacitance variation with applied voltage, the circle indicating the point of instability (pull-in) at 3.3 V**

Loss measurement of the varactor has been carried out using Vector Network Analyser. The return loss and insertion loss of this varactor at zero voltage are plotted in Fig 24.



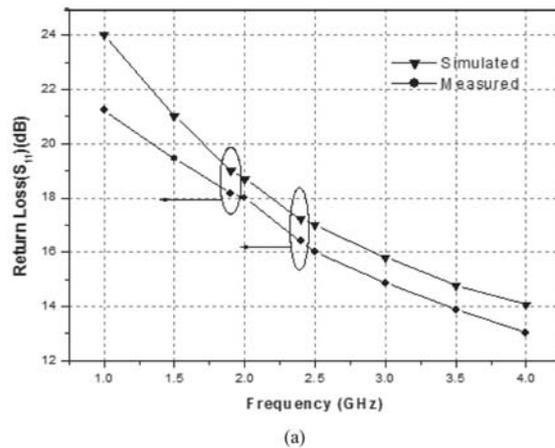
(a)



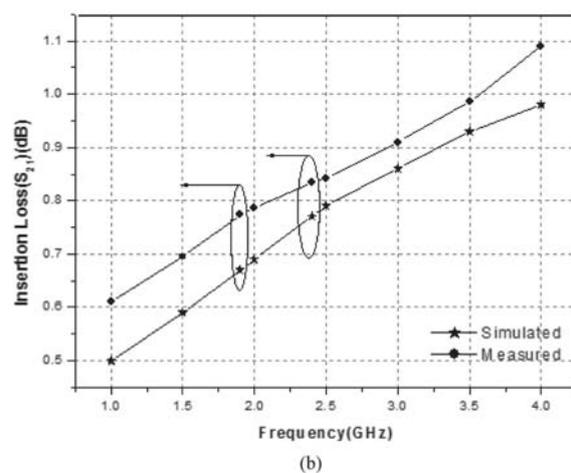
(b)

**Figure 22 (a) Vibration spectrum of the MEMS varactor (b) First mode of vibration**

From the measured capacitances, the minimum and maximum capacitances available from the device are 0.86 pF and 0.896 pF, respectively.

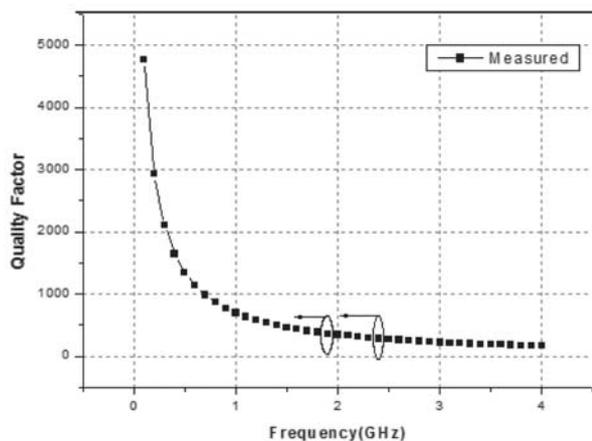


(a)



(b)

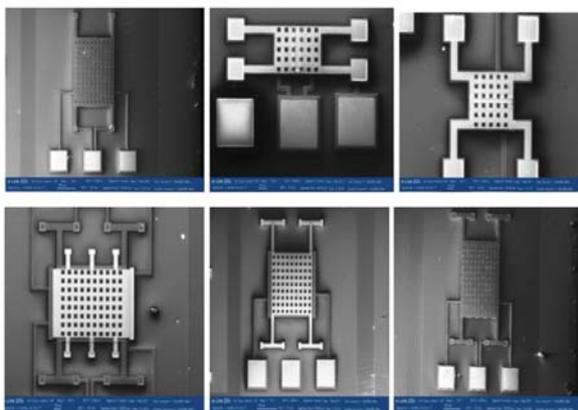
**Figure 24. (a) Return loss (b) Insertion Loss. Circles indicate return loss and insertion loss values at 1.9GHz and 2.4GHz.**



**Figure 25: Variation of quality factor with frequency. Circles indicate that the quality factor at 1.9 GHz=360 and at 2.4 GHz=280.**

This varactor is designed to integrate with the VCO, so loss analysis has been carried out up to 4 GHz. Return loss and insertion loss values are given at two different oscillation frequencies of the VCO; 1.9 GHz and 2.4 GHz. Quality factor values at these two frequencies are shown in Fig.25.

A few more varactors have been fabricated using PolyMUMPS process and shown in Fig. 26. Different meander-based configurations of the two-plate varactor have been developed and tested with mechanical, electrical, and RF performance analysis. The main objective behind this work is to achieve high quality factor along with a pull-in voltage of 3.3 V, which can be compatible with RFIC voltage-controlled oscillator (VCO).



**Figure 26 SEM of different meander based varactors fabricated using the polyMUMPS process**

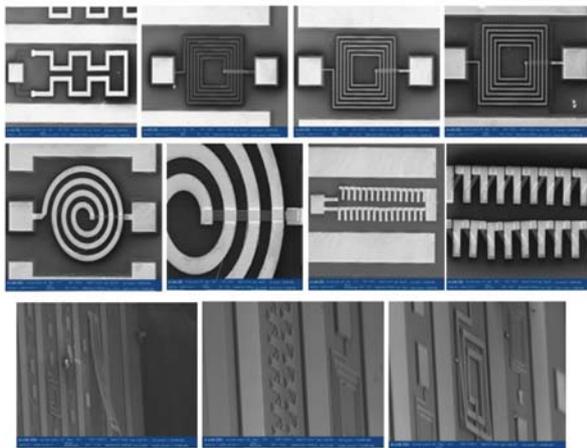
#### 4. RF inductor

RF inductors are needed in wireless front-end circuitry; the performance of both transceivers and

receivers depends heavily on this component. High-Q inductors reduce the phase noise and the power consumption of VCO's, self-adjusting matching networks or power amplifiers and reduce the return loss of matching networks and filters. The quality factor of inductors can be increased by using a thick metal layer [Pinel *et al.*, 2003], [Jiang *et al.*, 2000] and by isolating the inductor from the substrate [Chang *et al.*, 1993, Lakdawala *et al.*, 2002, Jiang *et al.*, 2000, Ribas *et al.*, 2000]. To isolate the inductor, bulk micromachining [Chang *et al.*, 1993, Lakdawala *et al.*, 2002, Jiang *et al.*, 2000, Ribas *et al.*, 2000, Yoon *et al.*, 2003] or self-assembly techniques [Dahlmann *et al.*, 2001], [Lubecke *et al.*, 2001] can be used. Further, tunable inductors allow for performance optimization of RF front-end circuits. To date, there has not been a practical implementation of a high-Q tunable inductor. Most of the reported MEMS inductors are static, fixed-value inductors. One variable inductor using MEMS switches has been reported [Chu *et al.*, 1993].

In general, tunable capacitors have better tuning range and quality factor (Q-factor) than tunable inductors. However, the tunability of the tunable inductors provides additional functionality, design flexibility and robustness, which make the tunable inductors promising for applications in the field of portable communication systems. Tunable inductors can be divided into four categories: discrete-tuned (DT), metal shielding-tuned (MST), magnetic core-tuned (MCT) and coil-coupled-tuned (CCT). The discrete-tuned inductor often uses micro-switches [Park *et al.*, 2004, Pham *et al.*, 2005, Lin *et al.*, 2005, Balachandran *et al.*, 2005] or micro-relays [Zhou *et al.*, 1997, Shifang *et al.*, 1997] to increase or decrease the effective coil length of the inductor, but the combination of the micro-switches or micro-relays will reduce the Q-factor of the inductor. The metal shielded tuned inductor is realized using moveable metal structure with large range, resulting in the change in magnetic flux of the inductor [Tasseti *et al.*, 2003]. The magnetic core-tuned inductor is realized using a solenoid inductor embedded with magnetic-core conductor, whose permeability can be changed by applying a magnetic field [Salvia *et al.*, 2005, Shih *et al.*, 2004]. The coil-coupled-tuned inductor mainly adjusts its mutual inductance between the primary coil and the secondary coil of the inductor [Tasseti *et al.*, 2004, Zine-El-Abidine *et al.*, 2005, Zine-El-Abidine 2005].

In our work, different types of spiral inductors have been fabricated using the polyMUMPs foundry process to check the performance in terms of inductance and quality factor. Figure 27 shows the SEM of some fabricated inductors.

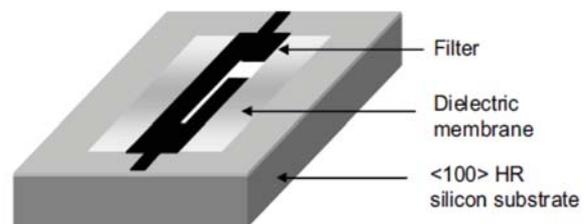


**Figure 27: MEMS Inductors fabricated using polyMUMPs process.**

## 5. RF mems filters

Among various RF circuits used in communication systems, band-stop filters are used to reject undesired frequencies. Furthermore, with the recent advances in microwave/millimeter-wave integrated circuits, there is a great demand of compact band-stop filters (BSF). Spur line filter embedded in 50-ohm transmission line is the potential candidate for compact filter realization. Schiffman and Matthaei [Schiffman *et al.*, 1964] first introduced spur line band-top filter in homogeneous medium. In 1977, Bates realized this filter in microstrip assuming same phase velocities for the even and odd modes [Bates *et al.*, 1977]. Later, Nguyen presented a detailed analysis considering unequal phase velocities of even and odd modes associated with inhomogeneous microstrip medium [Nguyen *et al.*, 1983]. Till now, many variants of spur line filter have been reported for wide-band and better rejection characteristics. Most of the reported work is on designing the filter on low-permittivity substrate such as RT-Duroid ( $\epsilon_r \sim 2.22$ ). But with the development of monolithic microwave integrated circuit (MMIC) technology, it would be advantageous if filters can be fabricated on high dielectric constant ( $\epsilon_r > 10$ ) substrates such as silicon and gallium arsenide. Microstrip filters fabricated on high dielectric constant substrates can

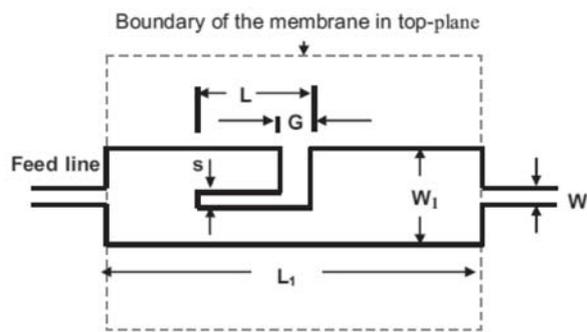
be easily integrated with MMIC RF front-end circuitry. The major factors that limits the performance of a filter fabricated on high-permittivity ( $\epsilon_r = 11.9$ ) silicon substrates are the high dielectric and radiation losses in the substrate that result in the reduced unloaded Q of the filter. A low unloaded Q of a filter results in high insertion loss and poor rejection performance. The silicon bulk-micromachining technique suppresses most of these drawbacks by replacing the substrate with a thin dielectric membrane. In bulk micromachining, the bulk silicon material is removed underneath the circuit as shown in Fig.28 to synthesize an artificial low dielectric constant ( $\epsilon_r = 1$ ) region around the circuit. In the past, micromachining has been successfully employed to realize K- and W-band microstrip filters [Chi *et al.*, 1996, Robertson *et al.*, 1996]. A three-layer membrane of dielectric stack of  $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ , obtained by bulk-micromachining of the high-resistivity  $\langle 100 \rangle$  silicon substrate is the key element in this work.



**Figure 28: Schematic of micromachined spur line band stop filter.**

Figure 29 shows the circuit board dimensions of the proposed micromachined spur line BSF. The middle portion of the filter, similar to feed line, is a 50-ohm transmission line on an air-suspended membrane. The spur line BSF with identical coupled lines in inhomogeneous microstrip configuration was designed using expressions given in [Schiffman *et al.*, 1964, Nguyen *et al.*, 1983, Bates *et al.*, 1977, Smith *et al.*, 1971].

The values for even and odd mode phase velocities i.e.,  $\epsilon_{oe}$ ,  $\epsilon_{oo}$  and  $s$  can be calculated by writing a computer program based on Smith's paper [Smith *et al.*, 1971]. In practice, the presence of a thin dielectric membrane slightly alters the value of the dielectric constant from that of air. Therefore, in the program, the permittivity  $\epsilon_r$  of the dielectric should be replaced by its equivalent value to account for a multi-layer dielectric stack (silicon nitride/air)



**Figure 29: Schematic layout of the spur line band-stop filter on micromachined silicon substrate.**

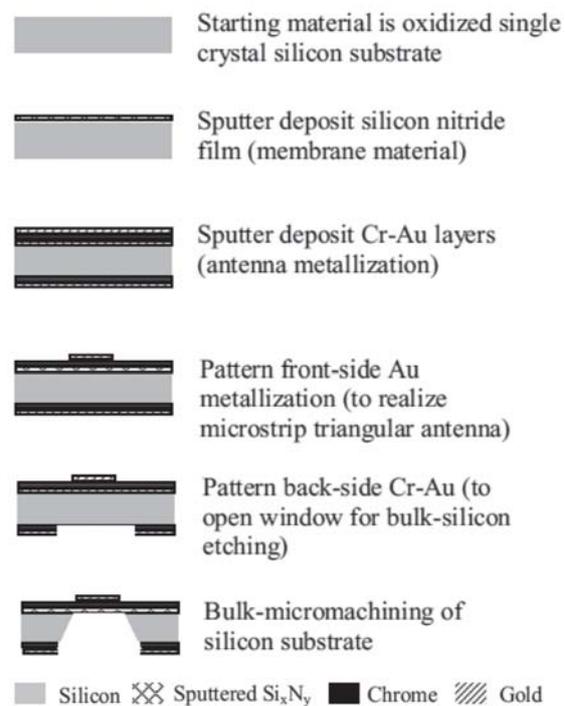
formed as a result of micromachining the bulk silicon. The filter structure was analyzed and optimized using the finite-element method (FEM)-based software, Agilent High Frequency Structure Simulator [HFSS version 5.5]. Table-III gives the dimensions of the filter designed with center frequency near 8.7 GHz on high resistivity ( $>3000 \Omega\text{-cm}$ ) silicon substrate.

**Table 3: Dimension of the spurline bsf on micromachined substrate**

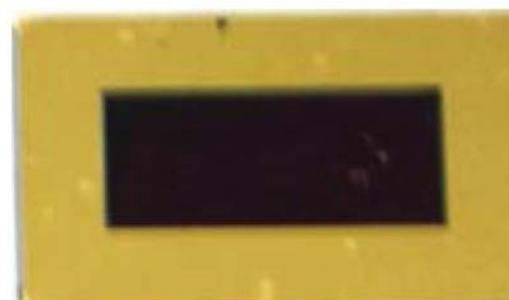
Functional Parameter	Value
L(mm)	7.9
G(mm)	0.3
S(mm)	0.2
$L_1$ (mm)	10
Lateral dimension of the cavity in top plane (mm $\times$ mm)	10 $\times$ 4.5
Lateral dimension of the cavity in bottom plane (mm $\times$ mm)	10.38 $\times$ 4.88
Width of the feed line W (mm)	0.2
Thickness of the silicon nitride layer ( $\mu\text{m}$ )	3
Thickness of the HRS silicon substrate (mm)	0.27

Fabrication of the filter starts with  $\langle 100 \rangle$  oriented high resistivity ( $>3000 \Omega\text{-cm}$ ) single crystal silicon substrate (HRS). To start with, a thin dielectric film of silicon nitride is deposited on silicon substrates by radio frequency (RF) sputtering. After patterning the filter conductor on top of the dielectric film, the dielectric membrane is released using bulk-micromachining technique. The process-flow adopted in realizing the micromachined RF circuit

is described in detail in [Sharma *et al.*, 2006]. The complete sequential process-flow for reference is shown in Fig. 30. The fabricated filter is shown in Fig.31.



(a)



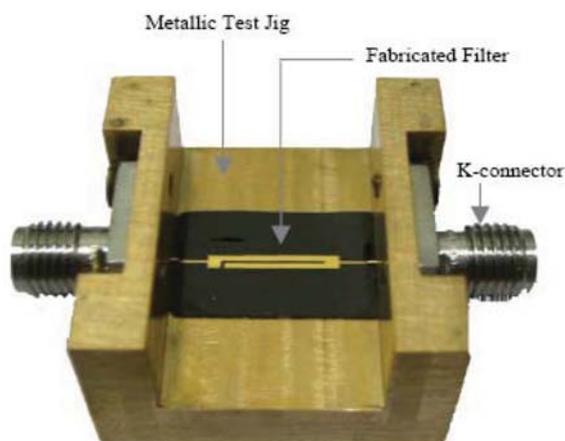
(b)

**Figure 31 Photographs of micromachined spur line band-stop filter (a) Front-side showing the conductor pattern (b) Backside showing the etched cavity.**

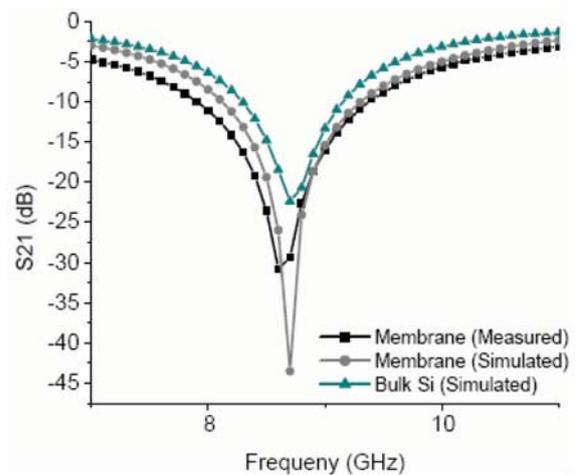
For testing, the fabricated filter was mounted on a test jig as shown in Fig. 32. The filter was excited using K- Connector (Tensolite model no. 230CCSF) to microstrip transition. The center frequency and bandwidth were obtained from reflection and transmission measurements. The S-parameters were measured on a Vector Network Analyzer (VNA) (Rhodes and Schwarz, Model ZVK-1127.8651.60). The VNA was calibrated from 5-13 GHz using TOSM standards. The measured transmission characteristics of the micromachined spur line BSF are plotted in Fig. 32.

The measured 10-dB rejection band of the spur line is 7.9-9.6 GHz and the deepest rejection level is better than 30 dB. The measured and simulated center frequencies are 8.6 and 8.7 GHz, respectively. For comparison, results of a spur line BSF designed on bulk silicon are also plotted in Fig. 32. It can be concluded that filter realized on thin dielectric membrane exhibits wide-band and better rejection characteristics as compared to filter realized on high-permittivity bulk silicon. As observed, the simulated and measured data agrees well.

Using silicon bulk-micromachining, a wide band spur line band-stop filter is proposed. The proposed BSF shows a deeper rejection level as compared to the BSF realized on bulk silicon substrate. The filter was fabricated using a CMOS compatible metal-dielectric deposition technique suitable for post CMOS MEMS processing.

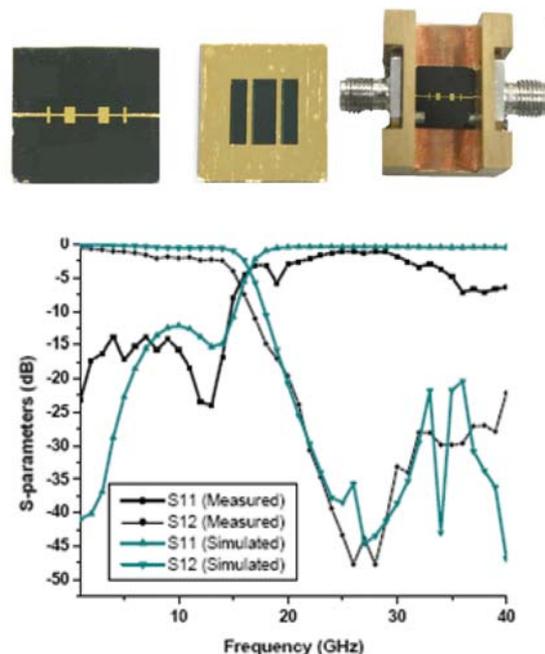


**Figure 32** Photograph of fabricated spur line BSF on micromachined substrate mounted on the test jig with K-connector launchers.

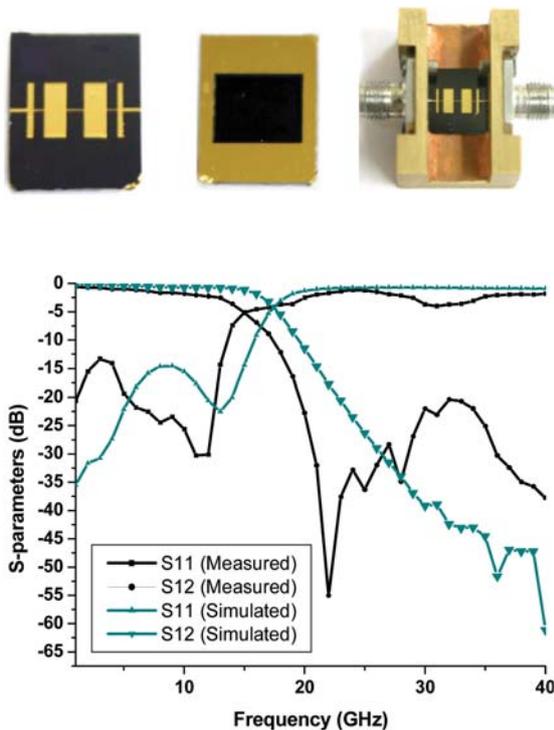


**Figure 33** Simulated and measured transmission characteristics of spur line BSF.

Several other types of filters that utilize the advantageous features of bulk- micromachining have also been fabricated. These include a low pass filter of the high-impedance, low-impedance type, and stub-line sharp cut-off filters. Figure 34 shows the photograph of a low-impedance, high-impedance low pass filter that utilizes bulk-micromachined cavities underneath the inductive lines to increase their impedance. The simulated and measured characteristics of this type of low pass filter are also plotted in the same figure.

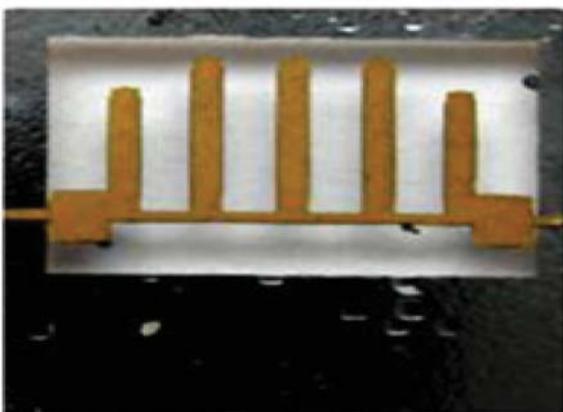


**Figure 34** Simulated and measured characteristics of low pass filter on silicon substrate with bulk micromachined cavities under inductive lines only.



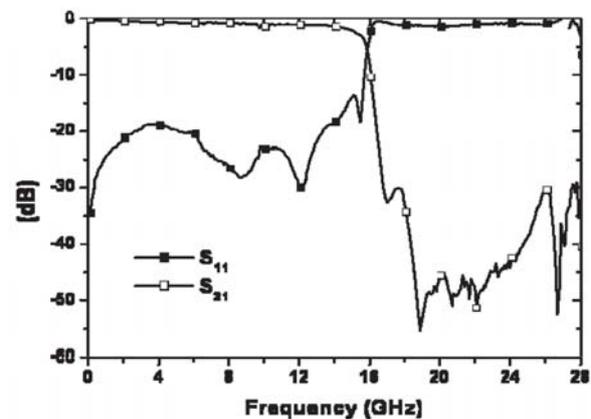
**Figure 35. Simulated and measured characteristics of low pass filter on silicon substrate with bulk micromachined cavities under inductive as well as capacitive lines.**

Figure 35 shows the photograph of a low-impedance high-impedance low pass filter that utilizes bulk-micromachined cavities under the inductive as well as capacitive lines. The simulated and measured characteristics of this type of low pass filter are also plotted in the same figure. As observed, good agreement is observed between simulated and measured results. Figure 36 shows the photograph of the stub line-type low pass filter



**Figure 36 Photograph of the stub line low pass filter fabricated on Silicon substrate using bulk-micromachining**

fabricated using bulk-micromachining on silicon wafer. The characteristics of this filter are plotted in Fig.37. As observed, the filter offers low insertion loss in the pass-band and sharp stop-band characteristics.



**Figure 37 Measured characteristics of stub line low pass filter on silicon substrate using bulk micromachining**

Compared with the filter fabricated on bulk silicon, insertion loss is very small and the stop-band characteristics are very sharp. The dimensions of the filter are also convenient for millimeter wave frequencies. Such filters should find application in the development of multiplexers at millimeter wave frequencies.

## 6. Mems phase shifter

The RFMEMS-based phase shifter is an important circuit element. Due to small size, low loss at RF frequencies, improved power handling capability, broadband operation, compatibility with traditional MMIC circuits, these are useful for a variety of applications. RF MEMS phase shifters can be used to realize MCM (multi-chip-module) and SOC (system-on-chip) with high-density package directly leading to overall size and weight reduction of a typical RF subsystem. The major parameters that define a RF and microwave phase shifter are centre frequency, bandwidth (BW), total phase variance ( $\Delta\phi$ ), insertion loss (IL), switching speed, power handling (P), accuracy and resolution, input/output matching (VSWR) or return loss (RL), and harmonic level.

There are different ways to implement the

RFMEMS phase shifter. Some of the most notable methods are based on Distributed MEMS Transmission Line (DMTL), switched-line, loaded line, and reflection type. Many research groups have concentrated on DMTL-based digital phase shifter. In a typical digital DMTL phase shifter, about eight RF MEMS switches are used to generate  $90^\circ$  phase shift and sixteen RF MEMS switches are needed for a  $180^\circ$  phase shift. Smaller number of switches will be required for lower phase bits. These switches are placed periodically over the transmission line. The length of the DMTL phase shifter is typically large as compared with other types reported. Range couplers in reflection-type phase shifters take up large chip area and increase the loss when using a high resistivity substrate. On the other hand, the switched-line configuration is the most straightforward approach that utilizes simple time delay difference between two direct paths to provide the desired phase shift [Jian *et al.*, 2006].

In this work, details of the development of 5 bit digital phase shifter with inline metal-metal contact MEMS series switch on CPW transmission line are presented. Gold-based surface micromachining process has been used to develop a complete 5-bit phase shifter.

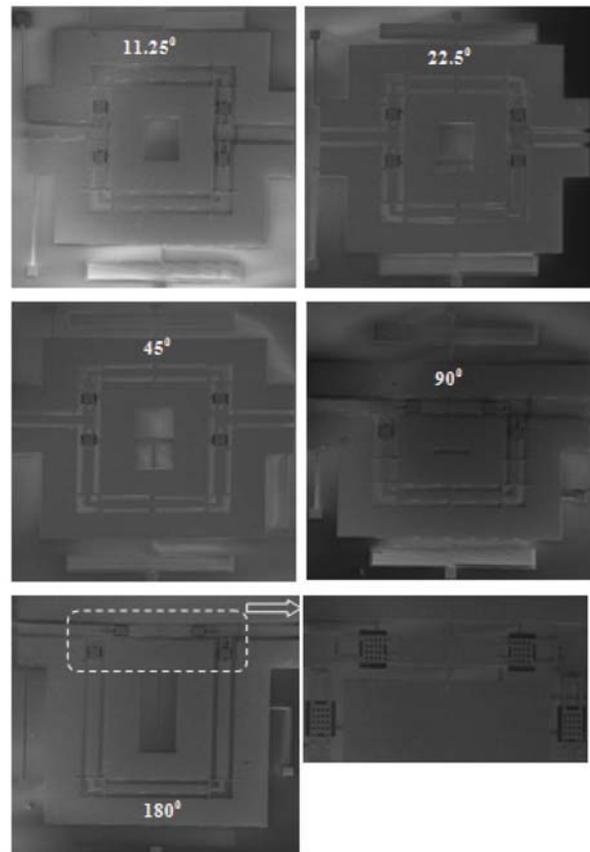
A 5-bit phase shifter comprises five primary bits:  $11.25^\circ$ ,  $22.5^\circ$ ,  $45^\circ$ ,  $90^\circ$  and  $180^\circ$  phase bits. All individual bits have been fabricated individually to get the desired phase response and then integrated into a complete 5-bit phase shifter. The design is based on SPDT switches where two SW1 MEMS switches are placed in a back-to-back configuration. Thus each section has only four MEMS switches. As the insertion loss of the phase shifter is mainly caused by conductors and switch losses, fewer switches can result in a low insertion loss. More detail description of this kind of phase shifter can be found in [Dey *et al.*, 2013].

MEMS switches are employed to route the input RF signal into the appropriate length of matched transmission lines. The phase shift of each bit is given by (19), [Jian *et al.*, 2006]

$$\Delta\phi = \frac{2\pi(l_d - l_r)}{\lambda} = \frac{2\pi f \sqrt{\epsilon_{eff}}(l_d - l_r)}{c} \quad (19)$$

where  $l_d$  and  $l_r$  are the lengths of delay lines and reference lines, respectively. The SEM images of individual switched line phase shifter bits are shown in Fig 38.

The length of the reference line for  $11.25^\circ$ ,  $22.5^\circ$ ,  $45^\circ$ ,  $90^\circ$  and  $180^\circ$  phase bits are  $1675 \mu\text{m}$ ,  $1675 \mu\text{m}$ ,  $1675 \mu\text{m}$ ,  $570 \mu\text{m}$  and  $570 \mu\text{m}$  respectively. Similarly, the length of the delay line for  $11.25^\circ$ ,  $22.5^\circ$ ,  $45^\circ$ ,  $90^\circ$  and  $180^\circ$  phase bits are  $1925 \mu\text{m}$ ,  $2150 \mu\text{m}$ ,  $2620 \mu\text{m}$ ,  $2480 \mu\text{m}$  and  $4320 \mu\text{m}$  respectively. A maximum return loss of better than 16.5 dB and a worst-case insertion loss of 1.05 dB have been obtained from individual phase bits in the frequency band from 13- 17.25 GHz, as shown in Figs. 39(a) – (e). The desired phase shift has nearly been achieved from individual phase bits with  $+0.79^\circ$  of phase error which is also validated through simulation, as shown in Fig 40.



**Figure 38 SEM images of five primary individual switched line phase shifter bits.**

Transmission lines with diode loading have been used for a variety of applications, both nonlinear [Rodwell *et al.*, 1991, Rodwell *et al.*, 1994] and linear [Zhang *et al.*, 1996, Nagra *et al.*, 1999]. In the linear regime, a diode-loaded line behaves like a synthetic transmission line where phase velocity changes with applied voltage and can, therefore, be used as true time delay (TTD) element in prototype phased arrays. TTD phase shifters are designed using the switched-line principle or the distributed loaded-line principle. In comparison with the switched-line, distributed phase shifter gives wide band performance, good aspect ratio and works well at higher frequencies. Distributed loaded-line TTD phase shifters can be realized analogously or digitally, and in smaller form factors, which is important at sub-array level. Analog phase shifters are biased with a single bias line, whereas digital phase shifters require a parallel bus along with complex routing schemes at the sub-array level. Practical phased arrays often require high isolation in phase control, which often leads to a large and lossy digital phase shifter system. In addition use of analog phase shifter in a sub-array avoids large phase quantization errors, which degrade the effective isotropically radiated power (EIRP) and beam-pointing accuracy, and elevate the side-lobe level of an electronically scanned array [Brookner., 1991, Mailloux., 2005]. In the present work, an analog DMTL TTD phase shifter has been chosen for phased array applications

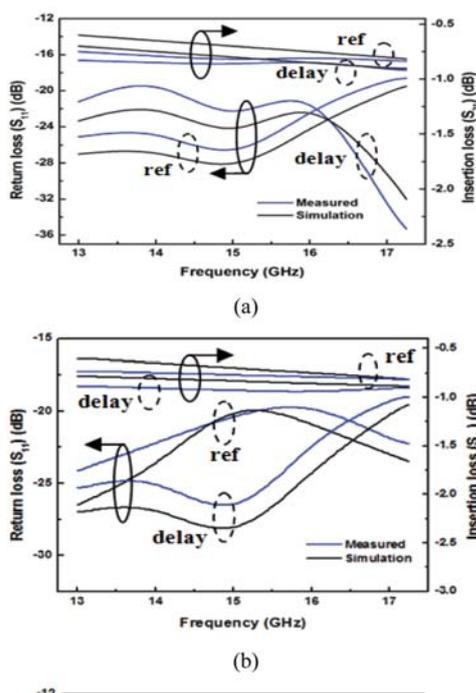


Figure 39 Measured versus simulation results of individual-bits of the phase shifter (a) 11.25°, (b) 22.5°, (c) 45°, (d) 90° and (e) 180°

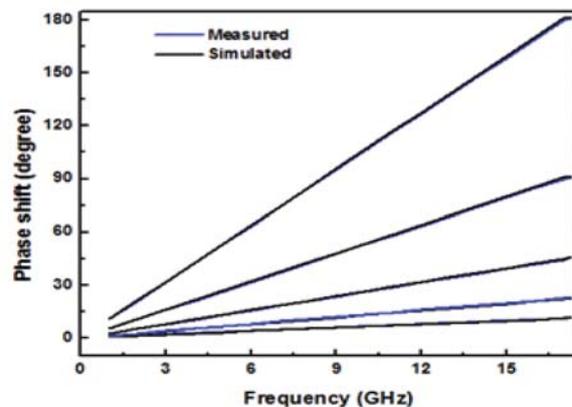


Figure.40 Measured and simulated phase shift versus frequency of individual phase-bits.

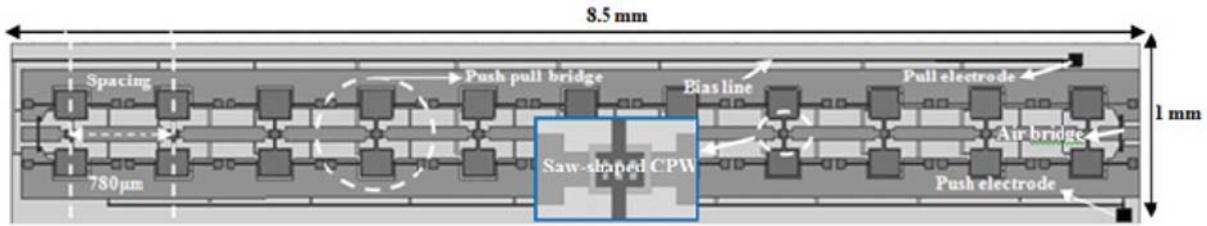
In general, DMTL consists of a coplanar waveguide (CPW) line that is periodically loaded with MEMS bridges. CPW-based phase shifters are uniplanar, as only one side of the substrate is used, eliminating the need for via-hole process and simplifying the fabrication and integration process with other components. When a single analog control bias voltage is applied to the centre conductor, the bridges will be pulled closer to the centre conductor which, in turn, increases the loading capacitance on the distributed line, apart from varying the propagation characteristics and decreasing the phase velocity of the DMTL. The resulting change in the phase velocity of the DMTL produces the TTD phase shift.

The DMTL design has been demonstrated from the X- to the W-band. Barker and Rebeiz [Rebeiz., 2003] were among the first who proposed and studied the MEMS distributed phase shifter. Later, further improvements in phase shifter were reported by other researchers [Borgioli *et al.*, 2000, Hayden *et al.*, 2000, Hayden *et al.*, 2001, Lakshminarayanan *et al.*, 2002]. A one-bit low-loss phase shifter was developed with 180° phase shift at 25 GHz and 270° at 35 GHz [Borgioli *et al.*, 2000]. Lakshminarayanan *et al.*, [Lakshminarayanan *et al.*, 2002] reported a phase shifter with figure of merit of 240°/dB at 35 GHz with return loss better than 10 dB from 10 to 35 GHz. [McFeetors *et al.*, 2006] presented DMTL analog phase shifter with enhanced tuning where a 225°/dB figure of merit has been achieved at 40 GHz. In [Wu *et al.*, 2007], a DMTL phase shifter has been developed using saw-shaped CPW, where a 20 dB return loss has been obtained with 90° phase shift at 10 GHz. In [Solazzi *et al.*, 2010], a symmetric toggle MEMS varactor, designed by [Rangra *et al.*, 2005], was used to obtain a 360° phase shift at 35 GHz with a return loss of 15 dB. In [Caekenbergh *et al.*, 2008], an analog slot line TTD is reported with 28.2°/dB and 59.2°/cm phase shift at 10 GHz. Prior studies have dealt with the structure design of the phase shifters in order to improve the phase shift per decibel noise figure (NF). However, the research work has not been extensive and the dependence of mechanical and electrical properties on various structural parameters is still an active area of research. Most of the reported phase shifters so far report the use of a high actuation voltage. Achieving a high phase

shift per decibel NF at high frequency with low actuation voltage is still an active area of research. Furthermore, for any device to be used in a practical application, it must be reliable. In addition, for use in practical systems, proper package of the device needs to be looked into.

To improve the reliability of TTD phase shifter, it is always desirable to operate a MEMS bridge within a limit of instability where electrostatic force equals the restoring force of the MEMS bridge. So, it is recommended to actuate a MEMS bridge within the pull-in limit. To obtain the maximum phase shift with the minimum insertion loss over a wider band, the height of the MEMS bridge is always controlled within the 2-5  $\mu\text{m}$  range. This leads to a high actuation voltage, since the conventional design approach for phase shift change is the adjustment of the height of the MEMS bridges. However, the displacement of the bridge's height is limited for a certain frequency application and the capacitance ratio ( $C_p$ ) is small, leading to small phase shift. In order to increase  $C_p$ , it is necessary to use an insulation layer on the centre conductor under the bridges so as to achieve high capacitance in the down state. On the other hand, in order to maintain an acceptable matching over a wide band, it is recommended not to overload the transmission line with an excessively large MEMS capacitance in the down state. However, many researchers have used the centre conductor as a bottom electrode of the bridge and to pull the bridge completely down onto this layer on the dielectric leads to dielectric charging. It can cause the switch to either remain stuck after removal of the actuation voltage or failure to contact under the application of the pull-in voltage. It degrades the life time of the phase shifter as life time is a function of the applied voltage and the contact quality between the bridge and the dielectric. Earlier studies of the TTD phase shifter have dealt with the maximum amount of phase shift with the minimum insertion loss with high actuation voltage (>25V).

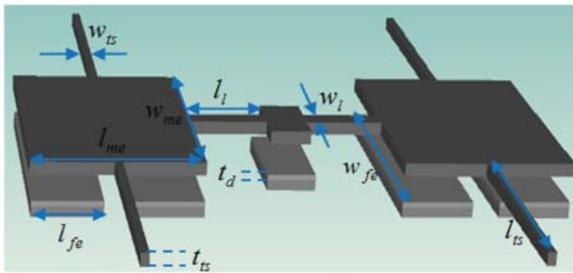
The present work focuses on developing a phase shifter that yields the maximum phase shift with the minimum actuation voltage, along with improvement in the return loss characteristics of the TTD phase shifter. Improvement in actuation voltage and switching time is always an active area of research in MEMS devices. Switching time is



**Figure 42** Layout of complete TTD phase shifter, inset shows the saw-shaped CPW. Complete area of the phase shifter is  $8.5 \text{ mm}^2$ .

not an important issue in a phase shifter if it operates within the pull-in limit. But, low actuation voltage sometimes effects device reliability. This paper attempts to address these points through analysis of the TTD phase shifter with low actuation voltage and a complete phase shift, along with good return loss characteristics. More detail description of this kind of phase shifter and its actuation principle can be found in [Dey et al., 2012].

The 3D image of a push-pull bridge is shown in Fig.41 with relevant device parameters.



**Figure.41** 3D model of the push-pull MEMS bridge.

The initial design parameters and material properties of the MEMS push-pull bridge are reported in Table IV and Table V, respectively.

**Table 4: Dimensions of the micromachined push-pull actuator**

Functional Parameter	Value ( $\mu\text{m}$ )
Fixed electrode length	90
Fixed electrode width	230
Mobile electrode length	200
Mobile electrode width	230
Lever length	85
Lever width	20
Length of the torsional spring	190
Width of torsional spring	15
Thickness of torsional spring	1.25
Thickness of lever	1.25

**Table 5: Material properties of push-pull type MEMS bridge**

Functional Parameter	Value ( $\mu\text{m}$ )
Layer for the mobile plate and fixed plate	$1.25 \mu\text{m}$
Thickness of the layer and the plate, $t_{me}$	$2.5 \mu\text{m}$
Initial distance between the fixed and the mobile electrode, $g_0$	
Conductivity of plate material,	$4.1 \text{ e}^7 \text{ S/m}^*$
Density of the plate material,	$19300 \text{ kgm}^{-3}$
Young's modulus of the plate material, $E$	$45 \text{ GPa}^*$
Poisson's ratio of plate material, $\delta$	$0.41^*$
Sheet resistance of fixed plate	$0.02 \text{ ohm}^*$
Sheet resistance of mobile plate	$0.025 \text{ ohm}^*$
Dielectric layer, $\text{SiO}_2$	$0.5 \mu\text{m}$
Dielectric thickness, $t_d$	$4^*$
Relative permittivity of dielectric,	11.9

The model for a TTD unit cell has three operating states, push-, up- and pull-state. In the up-state, the model comprises a transmission line of length  $s$ , with capacitor to ground due to shunt bridge ( $C_{up}$ ) and impedance is  $Z_{up}$ . In the push-state, central part of the beam is lifted upward under  $V_{push}$ , leading to increased loaded impedance ( $Z_{lpush}$ ) with low capacitance ( $C_{push}$ ). In the pull-state, bridge moves down within the pull-in limit, up to a gap height of  $0.75 \mu\text{m}$  from zero bias state, leading to decreased loaded impedance ( $Z_{lpull}$ ) with high capacitance ( $C_{pull}$ ).

The impedance for each state of the unit cell is given by (20), as follows [Rebeiz., 2003]

$$Z_{up} = \sqrt{\frac{sL_t}{sC_t + C_{up}}} \quad Z_{push} = \sqrt{\frac{sL_t}{sC_t + C_{push}}} \quad Z_{pull} = \sqrt{\frac{sL_t}{sC_t + C_{pull}}} \quad (20)$$

where  $L_t$  and  $C_t$  are the inductance and capacitance per unit length .

These are given in (21) [Rebeiz., 2003]

$$C_t = \frac{\sqrt{\epsilon_{eff}}}{cZ_0}, \quad L_t = C_t Z_0^2 \quad (21)$$

Here,  $\epsilon_{eff}$  is the effective dielectric constant of the transmission line,  $Z_0$  is the unloaded line impedance and  $c$  is the free space velocity.

In order to maintain acceptable matching over a wide band, it is recommended not to overload the transmission line with an excessively large MEMS capacitance. In this circuit, saw-shaped centre conductor is used at the place where the MEMS bridge is built, to reduce the overlapping area. This leads to a reduction of the down-state impedance.

$C_{push}$ ,  $C_{up}$  and  $C_{pull}$  can be obtained using the parallel plate approximation, as given in (22)

$$C_{push} = \frac{\epsilon_0 w_{cb} W_1}{g_1 + \frac{t_d}{\epsilon_r}} + C_f \quad C_{up} = \frac{\epsilon_0 w_{cb} W_1}{g_0 + \frac{t_d}{\epsilon_r}} + C_f$$

$$C_{pull} = \frac{\epsilon_0 w_{cb} W_1}{g_2 + \frac{t_d}{\epsilon_r}} + C_f \quad (22)$$

The TTD phase shifter has a cut-off frequency called Bragg frequency ( $f_B$ ) near the point where almost total reflection occurs and impedance becomes zero with no power transfer.

For this reason, the Bragg frequency should be considered carefully to determine the upper operational frequency limit.

The Bragg frequency for the unit cell is given by (23) as follows [Rebeiz., 2003]

$$f_B = \left[ \pi \sqrt{sL_t (sC_t + C_b)} \right]^{-1} \quad (23)$$

where  $C_b$  is the bridge capacitance.  $g_1$  is the maximum travel range when beam is lifted upward under  $V_{push}$  and  $g_2$  is the

effective gap from top or zero bias state, within the pull-in range (considered to be  $0.75\mu\text{m}$  in this work) under  $V_{pull}$ .

The spacing ( $s$ ) and bridge capacitance ( $C_b$ ) (three states, push, up and pull) of the shunt beam is then calculated by rearranging (23) and is given in (24) as follows

$$s = c \left( \pi f_B \sqrt{\epsilon_{eff}} \right)^{-1}$$

$$C_{push} = s \left[ \frac{L_t}{Z_{push}^2} - C_t \right], \quad C_{up} = s \left[ \frac{L_t}{Z_{up}^2} - C_t \right], \quad C_{pull} = s \left[ \frac{L_t}{Z_{pull}^2} - C_t \right] \quad (24)$$

It is seen from (24) that  $s$  is inversely proportional to  $f_B$  and the  $\epsilon_{eff}$  of the substrate.

Using (21)-(24), the phase constants in each state ( $\beta_{push}$ ,  $\beta_{pull}$ ) and the net phase shift ( $\Delta\phi$ ) are derived. The final expressions are given in (25) as follows:

$$\beta_{push} = \frac{360}{2\pi} s \omega \left[ \sqrt{L_t C_t \left( 1 + \frac{C_{push}}{C_t} \right)} \right]$$

$$\beta_{pull} = \frac{360}{2\pi} s \omega \left[ \sqrt{L_t C_t \left( 1 + \frac{C_{pull}}{C_t} \right)} \right]$$

$$\Delta\phi = \beta_{push} - \beta_{pull}$$

$$= \frac{360}{2\pi} s \omega \left[ \sqrt{L_t C_t \left( 1 + \frac{C_{push}}{C_t} \right)} - \sqrt{L_t C_t \left( 1 + \frac{C_{pull}}{C_t} \right)} \right] \quad (25)$$

upward; so, the phase constant ( $\beta_{push}$ ) decreases due to the smaller loading capacitance ( $C_{push}$ ). This leads to a high loaded impedance ( $Z_{push}$ ). The centre beam gets downward deflection in the pull state and that leads to a higher phase constant ( $\beta_{pull}$ ) due to a higher loading capacitance ( $C_{pull}$ ) with low loaded impedance ( $Z_{pull}$ ). Therefore, the difference in the phase constants ( $\Delta\phi$ ) between the two states increases.

Total travel range ( $TTR$ ) of push-pull TTD phase shifter is given in (26), as follows:

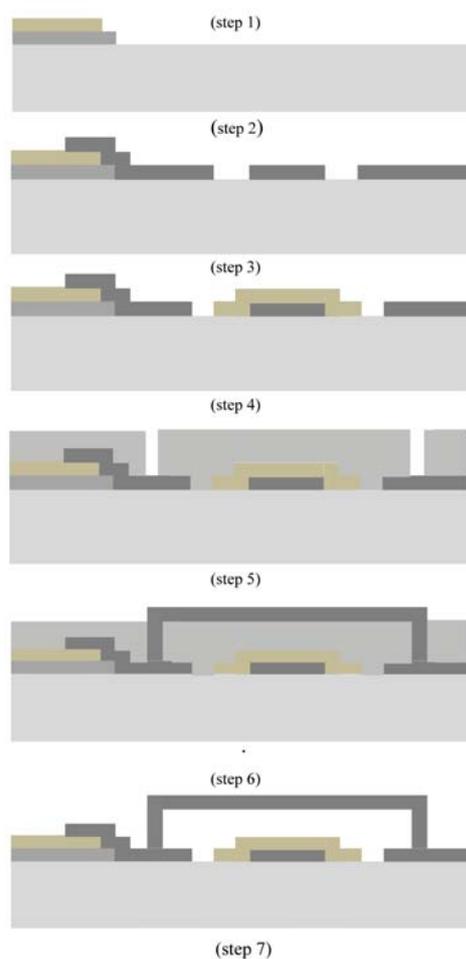
$$TTR (\mu\text{m}) = g_1 + g_2 = 3.81 + 0.75 = 4.56 \quad (26)$$

Capacitance ratio ( $C_r$ ) of push-pull type MEMS bridge is given in (27):

$$C_r = \frac{C_{pull}}{C_{push}} \quad (27)$$

The first phase of our work focussed on the development of the unit cell of the phase shifter. The second phase deals with the repetition of unit cell with constant spacing to make a complete TTD phase shifter. The layout of the DMTL TTD phase shifter has been drawn in the CoventorWare layout editor platform where 11 unit cells are periodically placed with 780  $\mu\text{m}$  spacing, as shown in Fig.42. All fabrication details and experimental observation can be found in [Dey *et al.*, 2012], although all relevant results are cited here for reader benefit.

The fabrication process requires six masks and consists of the steps shown in Fig. 43. The process of push-pull TTD phase shifter starts with a 0.025"-thick alumina substrate polished on both sides.

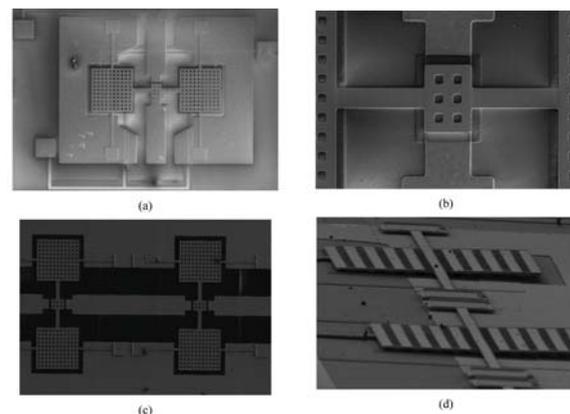


**Figure 43 Schematic showing micro-fabrication process steps.**

**Step 1.** After the RCA cleaning of the wafer, the first layer of chromium (Cr) is deposited and patterned using the lift-off technique. This layer is used for electrical biasing in the circuit by mask 1.

**Step 2.** A 0.3  $\mu\text{m}$  layer of silicon oxide ( $\text{SiO}_2$ ) is deposited using plasma enhanced chemical vapour deposition (PECVD) and patterned. RIE is employed to pattern the oxide and remove the patterning photo resist. This is a passivation layer and deposited on the last layer (Cr) by mask 2. The sheet resistance of this layer is 0.025  $\Omega/\text{sq}$ .

**Step 3.** An evaporated 400  $\text{\AA}$  chromium/100 nm gold bi-layer is deposited as a seed layer. A photo-resist mould is formed in the third lithographic step and 1  $\mu\text{m}$  gold is electroplated inside the mould. The mould and seed layers are removed afterwards. Chromium is applied as an adhesion layer for the



**Figure 44 SEM Images of Micro-fabricated push-pull TTD phase shifter. (a) Unit cell TTD phase shifter (b) Close view of contact beam (c),(d) Top and cross section view of consecutive two bridges with periodic placement (780  $\mu\text{m}$ ) on distributed TTD phase shifter**

gold. This layer is used to pattern the CPW line, fixed electrodes and bias pad by mask 3.

**Step 4.** A 300  $\text{\AA}$  of Titanium Tungsten (TiW) film is sputtered, followed by the deposition of 0.5  $\mu\text{m}$  silicon oxide using PECVD at 250 $^{\circ}\text{C}$ . The dielectric and TiW layers are dry etched. The TiW layer serves as an adhesion layer for the silicon oxide to the gold. This layer is patterned by mask 4 to make an insulation layer on CPW line and on actuation electrodes.

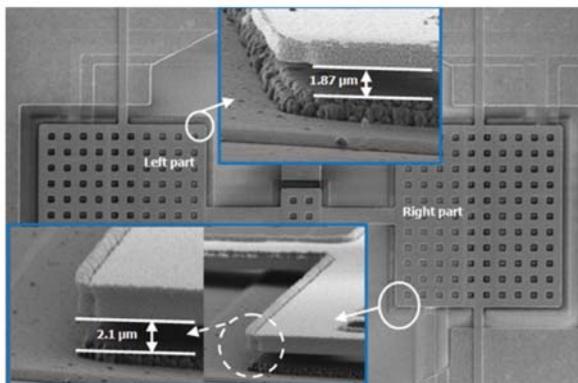
**Step 5.** Spin-coated polyimide (PI) is used as the sacrificial layer for this process. Initially, it is coated to a thickness of 2.5  $\mu\text{m}$ . Next, it is patterned by

mask 5 (anchor mask) in an RIE step to etch the PI and fully clear the anchor holes.

**Step 6.** The top gold layer consists of a sputtered gold seed layer and an electroplated gold. The total thickness of this layer is  $1.25\ \mu\text{m}$ , and used as the structural layer for the devices. Moulding method is used to define this layer. This layer is patterned to make mobile electrode by mask 6. The sheet resistance of this layer is  $0.02\ \Omega/\text{sq}$ .

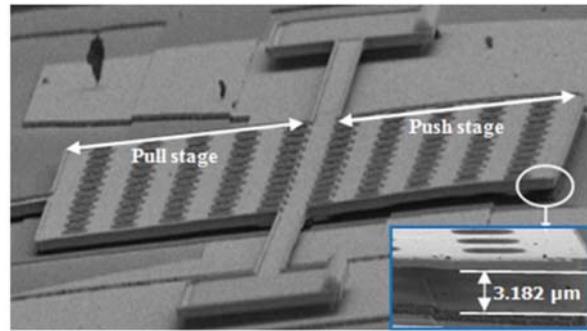
**Step 7.** The last step is the release process. In this process, the sacrificial layer is removed in an oxygen plasma dry etch process.

Micro-fabricated images of a TTD phase shifter are shown in Fig. 44. Initial deformation of the MEMS bridge after removal of polyimide sacrificial layer has been measured through SEM. Non-uniform distribution of gap height has been captured on the mobile plate between two different sides (left and right) of pull and push stages over separated bottom electrodes along with the centre part of the bridge.

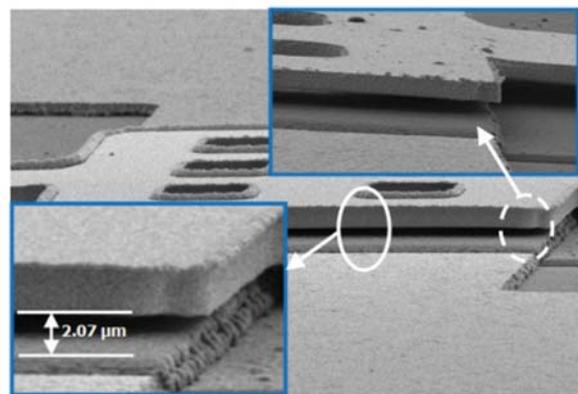


**Figure 45** Initial deformation of left and right parts of the mobile plate over the pull electrodes; inset shows the deformation.

Mobile plate deforms downwards over pull stage and lifted upward over push stage. It happens due to the asymmetric nature of the push-pull bridge configuration. Push stages are buckled up as it can't release the stress. However, process residual stress is  $\sigma_0 = 110\ \text{MPa}$ . Furthermore, this residual stress is tensile ( $\sigma_0 > 0$ ) in nature, while a compressive stress ( $\sigma_0 < 0$ ) induces buckling on the top plate over the push stage. Initial deformation of right and left sides of the mobile plate over the pull electrodes are  $0.63\ \mu\text{m}$  ( $1.87\ \mu\text{m}$  gap) and  $0.4\ \mu\text{m}$  ( $2.1\ \mu\text{m}$  gap), as shown in Fig.45. Average deformation over



**Figure 46** Initial deformation of push stage mobile electrode; inset shows the deformation.

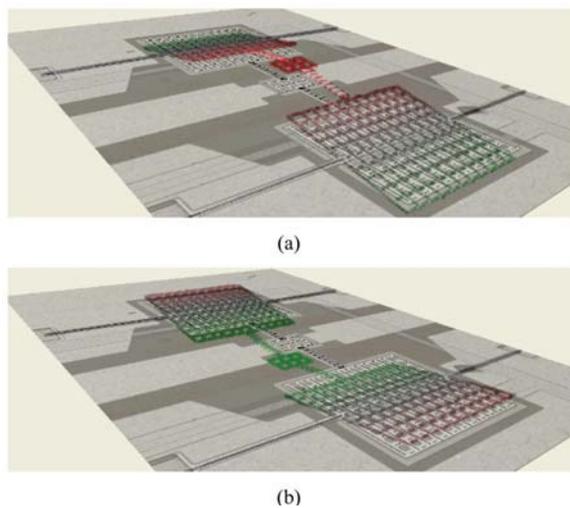


**Figure 47.** Initial deformation of the middle part of the bridge; insets shows the deformation.

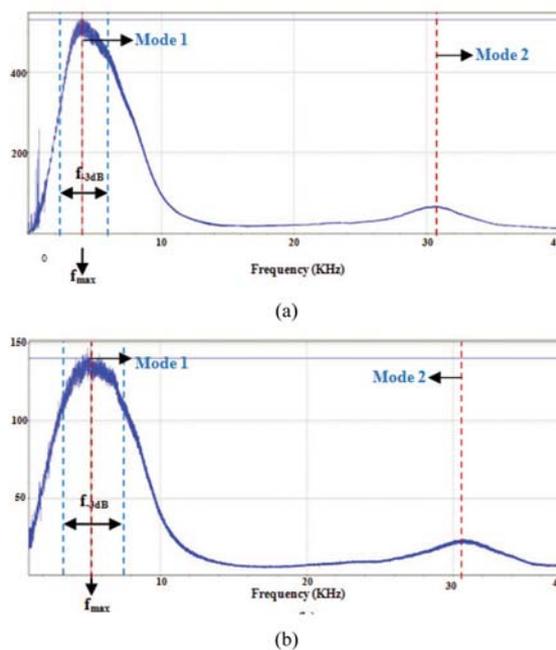
two stages of push stage is  $0.68\ \mu\text{m}$  ( $3.18\ \mu\text{m}$  gap), as shown in Fig.46. Furthermore, a  $0.43\ \mu\text{m}$  ( $2.07\ \mu\text{m}$  gap) downward deformation has been captured at the middle part of the beam over the separated signal line, as shown in Fig.47. Asymmetry of beam deformation introduces non-linearity into the structure, which affects the mechanical, electrical and loss performances of the push-pull bridge.

The push-pull bridge from unit cell of TTD phase shifter has been thoroughly characterized for mechanical response using a Laser Doppler Vibrometer (LDV). A wafer prober was utilized to provide electrical connection to the bridge, and two electrodes and a chirp voltage of frequency sweeping from 0 to 40 kHz was applied at the mobile electrode to excite out-of-plane vibration modes in the bridge membrane. The amplitude of the signal is set to 1 volt, smaller than the pull-in voltage of the push-pull bridge. The shapes of the fundamental mode of vibrations for two states of the push-pull bridge as obtained from the LDV measurement is shown in Fig. 48. It shows that the bridge is successfully released as it can perfectly move in

the out-of-plane direction without any surface tension or stiction. The vibration spectrum of the bridge with displacement as a function of frequency is shown in Fig. 49.



**Figure 48** Snapshot of the fundamental mode of vibration of the beam in two states. It clearly shows that the beam end freely moves in the out of plane direction under the actuation of (a) push electrodes, (b) pull electrodes.



**Figure 49** Vibration spectrum of the push-pull bridge; (a) pull state shows a resonance at 4.012 kHz (b) push state shows a resonance peak at 5.29 kHz.

The MEMS bridge lifted upward with 5.29 kHz resonance when the push electrode is excited as shown in Fig. 48(a). The bridge shows resonance at 4.012 kHz with the excitation of pull electrodes

as shown in Fig. 48(b). Modal frequencies have been verified through a sine wave signal with mode frequencies (5.29 kHz, 4.012 kHz) and the highest displacement has been extracted from LDV measurement. It ascertains the first mode of vibration of the push-pull bridge. Mode 2 has been observed at 31 kHz from both the states, as shown in Fig. 49.

The difference in the resonant frequencies between the push and pull states is due to stretching of the lever under excitation. In the push-pull bridge, the gap height is larger than the bridge thickness ( $t_b$ ), so that the maximum deflection at middle point is larger than  $t_b$ , considering the invalidity of small deflection. In the push stage, the beam moves up with the elongation of effective length of leverage due to the electrostatic effect, leading to increased effective spring constant ( $K_{effPush}$ ) in the overall structure. It introduces less damping and shifts the resonance frequency ( $f_{OPush}$ ) to a higher level. In the pull state, the central part of the beam bends down with a negligible increment of the effective spring constant ( $K_{effPull}$ ) with high damping, and leads to a decrease in the resonance frequency ( $f_{OPull}$ ).

To measure the C-V characteristics for the pull-state, the bottom fixed electrodes were grounded and the required voltage sweep from 0 volt to 10 volt applied to the top suspended or mobile electrode using the probes. A small AC signal of 5 MHz was imposed on the DC actuation voltage to measure the capacitance. Open circuit offset measurement corrections were made before recording the capacitance values.

Three steps of capacitance variation have been observed in the pull state, as shown in Fig. 50. Initial deformation of the mobile plate introduces asymmetry on the bridge actuation over the separated bottom electrodes. It has been observed that initial deformation of the mobile electrode with respect to the bottom fixed pull electrode is not equal in the two stages. Downward deformation of left part of the mobile plate over pull electrode is more compared to the other side, as observed in Fig.46.

Capacitance variation at the left side of the pull electrode is more compared to the other part at the same voltage excitation for the asymmetric gap

height. Due to this, a sudden change in capacitance variation has been observed with a voltage variation from 2 to 2.1 V, as shown in step1 (Fig.50). The bridge reaches the point of instability with voltage variation from 4.2 to 4.4 V, above which ( $>4.5$  V), it completely snaps, as shown in step2. Non-uniform distribution of gap height over the mobile plate, along with the effect of stress-stiffing, leads to two steps pull-in as defined by step2 and step3. The non-uniformity may depend on the different positions of the dielectric-membrane contact points, and on the non-uniformity of the dielectric-membrane gap. One explanation of this voltage shift would be the effect of dielectric charging during step3, as the bottom electrode is insulated with a dielectric. Due to the high electric field, laterally inhomogeneous distribution of charge can be injected into the dielectric. The trap charges change the electric field and this leads to shift in the C-V curve to step3 with built-in voltage. This built-in

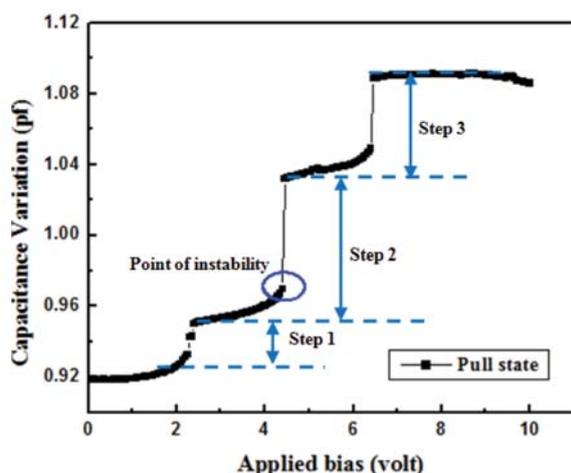


Figure 50 Capacitance versus voltage variations at Pull-state.

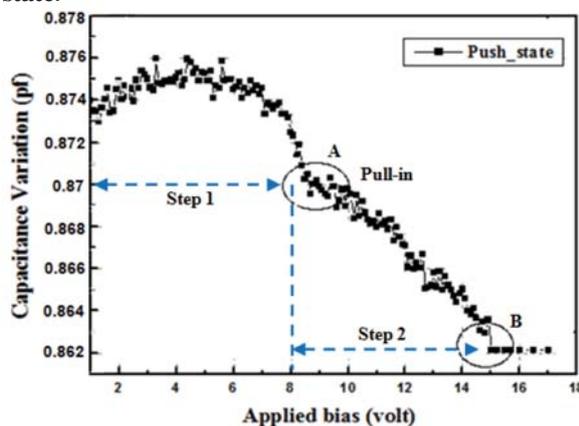


Figure 51 Capacitance versus voltage variation under push state.

voltage is proportional to the amount of charge, and to the distance between the trapped charge and the fixed bottom pull electrodes. The primary effect of such trapped charge is to shift the whole C-V characteristic towards positive of the voltage axis due to negative charge induction into the dielectric layer. However, there is another possible explanation of shifting the C-V curve from step2 to step3. This could be because of reduction of the gap due to mechanical degradation of the springs when the bridge is stressed. So, the narrowing effect of C-V curve at step3 can be avoided with controlled actuation voltage up to the point of instability ( $<4.4$  V).

In the push-state, the mobile electrode moves up with applied bias. It has been observed that mobile plate lifted up by  $0.68 \mu\text{m}$  from the initial gap height ( $2.5 \mu\text{m}$ ) over the push electrode (Fig.51). A voltage sweep from  $0 - 17$  V was imposed on the mobile electrode with reference to the fixed ground electrodes. A noticeable decrement of capacitance was captured through LCR meter, as effective gap height increases with applied DC bias.

The non-uniform profile of the beam introduces a very slow change in capacitance with a voltage variation up to  $8.1$  V, as shown in step1 (Fig.51). Once it reaches  $8.2$  V (point A), the beam

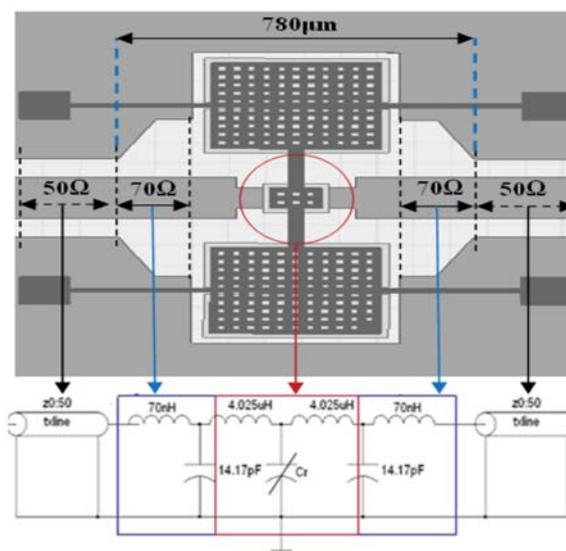
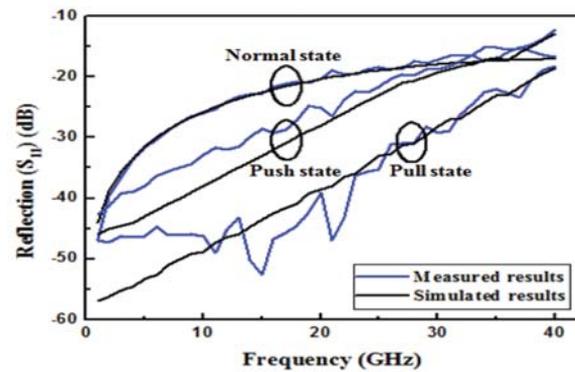


Figure.52 Schematic top view of unit cell phase shifter with equivalent circuit model; red circle indicates the red block in circuit model and blue arrows indicates the blue blocks.

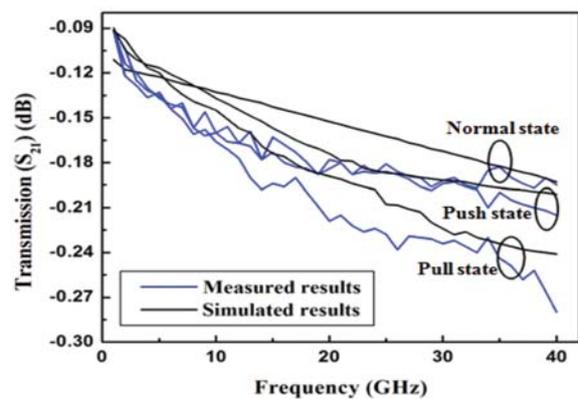
encounters the point of instability with a sudden decrement of capacitance (step2). The bridge moves up completely (point B) with a 15 V of actuation bias, followed by constant capacitance variation up to 17 V, as shown in Fig.51. The point of instability (pull-in) of the push-pull structure has been chosen to be 4.4 V in the pull state and 8.1 V in the push state to improve the repeatability over bridge actuation and to avoid dielectric charging effect over the insulated electrodes.

A CPW line is used as base transmission line with 70 nH/cm inductance and 14.17 pF/cm capacitance. This gives an unloaded characteristic impedance of 70  $\Omega$ , as shown in the equivalent circuit model of Fig.52. The line has a 100  $\mu\text{m}$ -wide centre conductor and 140  $\mu\text{m}$  gaps on the alumina substrate. The line is loaded with one MEMS bridge with a line length of 780  $\mu\text{m}$  to make a unit cell, which is the fundamental building block of complete distributed cell. An extra 200  $\mu\text{m}$  line of 50  $\Omega$  (width = 100  $\mu\text{m}$ , gap = 45  $\mu\text{m}$ ) has been kept in either side of the unit cell to start with the RF measurement, as shown in Fig.52. The MEMS bridge loads this line with 0.205 pF/cm capacitance ( $C_{up}$ ) along with 28.38 pH bridge inductance and 0.37  $\Omega$  resistance series with  $C_{up}$  at zero bias condition. The centre conductor is narrowed (saw-shaped) where MEMS bridge is loaded, and then an inductance (4.02 nH) is introduced on the transmission line on either side of the variable capacitance ( $C_p$ ), as shown in Fig.52.

The electromagnetic properties of the push-pull bridge were extracted from S-parameter measurements, by using a simple equivalent circuit model where the membrane works as a variable capacitance ( $C_p$ ) between push to pull state, as shown in Fig.52. In the push state, MEMS bridge is lifted upward and loads the line with 55.6 fF/cm capacitance under 8.1 volt push voltage. When a 4.1 V pull voltage is imposed on the electrode, the MEMS bridge moves down and loads the line with 0.589 pF/cm capacitance. To improve the reliability of the circuit, the bridge was actuated within point of instability (pull state < 4.2 V, push state < 8.2 V) in both the states. The designed up, push and pull state loaded impedances are 66.3  $\Omega$ , 69.28  $\Omega$  and 39.52  $\Omega$ , respectively. The Bragg frequency of the circuit is chosen to be 84 GHz.



(a)



(b)

**Figure 53 Measured versus simulated loss for a unit cell, (a) reflection (b) transmission.**

The push-pull TTD measurements and characterization were carried out with a HP8510C network analyzer and calibrated using the short-open-load-through (SOLT) on wafer standards. The measurement results of the unit cell with three different states have been validated using FEM-based simulation through HFSS and are plotted in Fig. 53. The reflection loss ( $S_{11}$ ) is better than 12 dB and a worst-case transmission loss ( $S_{21}$ ) of 0.28 dB has been obtained in the frequency band 1-40 GHz from the unit cell. The discrepancy between measured and simulated S-parameters is attributed to the overall height ( $g_0$ ) non-uniformities in the MEMS bridges that lead to asymmetric distribution of loaded line capacitances. A measured phase shift of 32.12° has been obtained from a unit cell. The figure-of-merit in degrees per decibel for the unit cell phase shifter is approximately 114.64°/dB at 40 GHz which is found to be within 5.4% of the simulation results (Fig.54). The CPW transmission line is loaded with 11 MEMS bridges with a spacing of 780  $\mu\text{m}$  to form a distributed loaded transmission line of 8.35 mm length. A return loss of better than

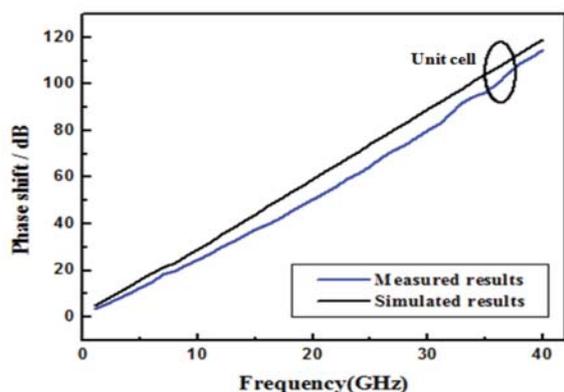
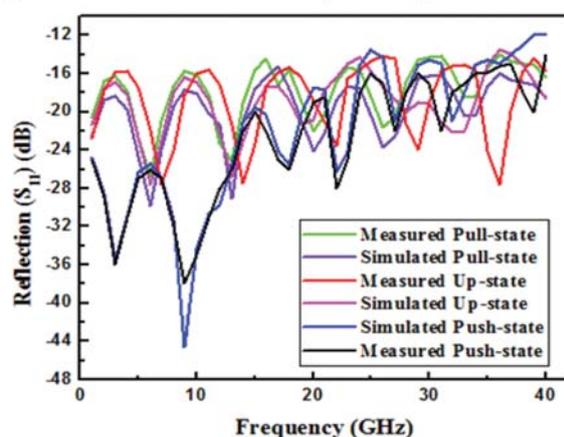
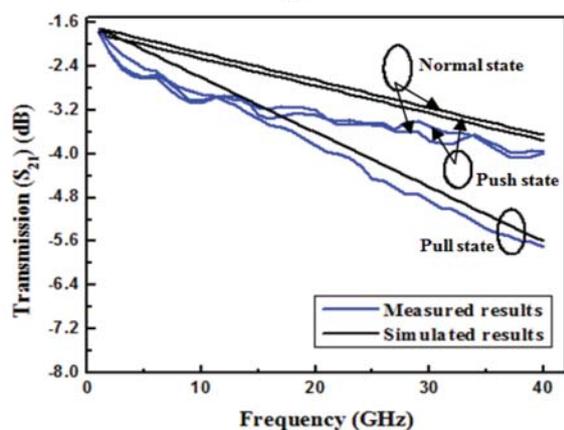


Figure 54 Measured versus simulated phase shift per dB



(a)

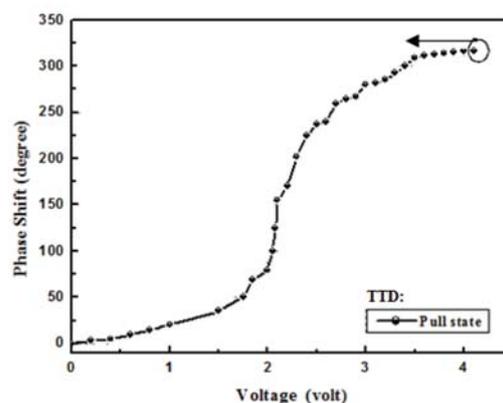


(b)

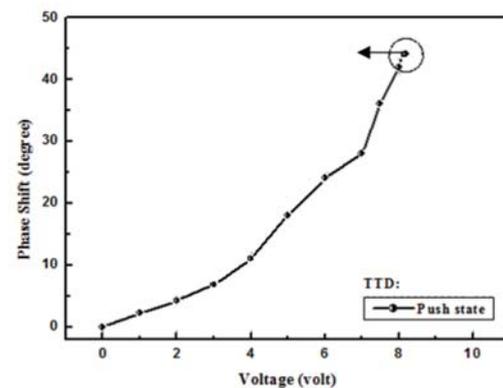
Figure.55 Measured versus simulated loss for distributed cell (a) reflection (b) transmission.

11.5 dB has been achieved up to 40 GHz as shown in Fig. 55(a). A maximum insertion loss of 3.75 dB has been noticed up to 20 GHz. Furthermore, it goes down to 5.7 dB at 40 GHz in pull states, as shown in Fig. 55(b). The agreement between measured and simulated insertion loss is found to be within 15% due to asymmetric distribution of gap profile throughout the TTD. Typical height non-uniformities

in the bridges are approximately 0.43-0.68  $\mu\text{m}$ . Furthermore, the increase in transmission loss ( $S_{21}$ ) of DMTL compared to the unit cell loss (0.28 dB) is due to the signal leakage via the Cr bias lines. The 36% reduction of bias resistance from 34.3 k $\Omega$  to 21.7 k $\Omega$  has been found from distributed cell to a unit cell.



(a)

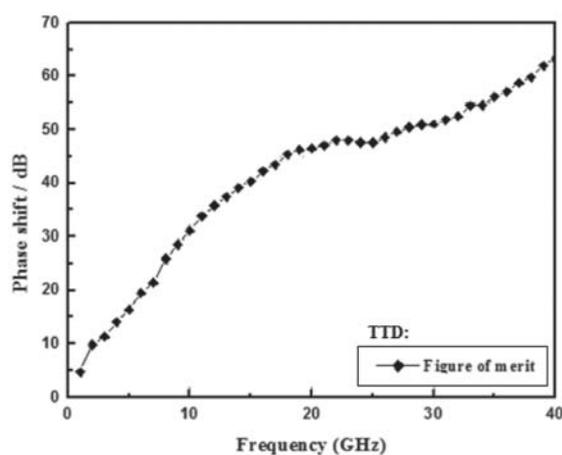


(b)

Figure 56 Measured variation of phase shift with applied bias; (a) pull state and (b) push state.

An analog version of the DMTL phase shifter has been designed for a maximum achievable capacitance ratio ( $C_{rp}$ ) of 10.5 within pull-in. Because the  $C_{rp}$  can be adjusted anywhere based on the voltage sweep, the phase shift which results can be considered analog due to the infinite number of states obtainable. The variation of phase shifts with applied bias for pull and push states with reference to the normal states have been recorded from VNA measurements and the results are shown in Fig.56. A phase shift of 317.15 $^\circ$ /cm has been obtained at 40 GHz with 4.1 volt actuation bias in the pull state, as shown in Fig.56. A sudden change in phase shift from 56 $^\circ$  to 152 $^\circ$  has been observed

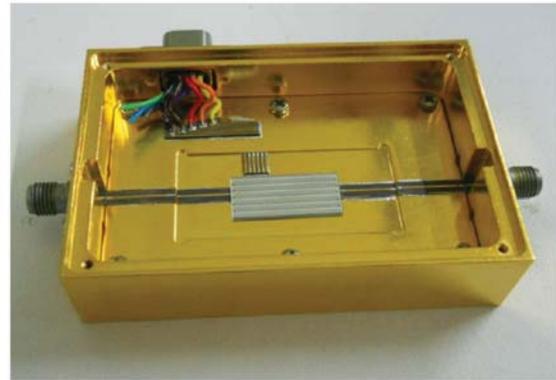
with a voltage variation from 2 to 2.1 V due to asymmetric gap distribution over the pull-electrode that leads to a change in the overall loaded line capacitance ( $C_{pull}$ ). This also validates Fig.50, where a noticeable change in capacitance has been captured with the same voltage transition from C-V measurement. In the push state, 44.1°/cm phase shift has been achieved with reference to the normal state at 40 GHz with 8.1 V actuation bias, as shown in Fig.56 (b). A continuous phase shift of 0 -360° has been obtained from the fabricated TTD device from push to pull state. A measured phase shift per



**Figure 57 Measured FOM performance of distributed cell.**

dB (63.25°/dB) has been obtained from the distributed cell at 40 GHz as shown in Fig.57. A novel topology for a TTD MEMS phase shifter with push-pull type bridge configuration has been implemented upto 40 GHz and presented in [[dey et al., 2012]]. The asymmetric nature of push-pull bridge and its effect on mechanical, electrical, and RF performance has been extensively investigated and validated to a reasonable extent. A figure of merit (FOM) of 114.64°/dB from an unit cell on alumina substrate has been achieved, which is the highest reported FOM at 40 GHz from a unit cell. The proposed device demonstrates complete differential phase shift of 0° - 360° up to 40 GHz with a minimum actuation voltage of 8.1 V.

In addition to the push-pull type of DMTL, conventional analog DMTL phase shifters have also been designed, fabricated and characterized. Figure 58 shows photograph of a DMTL phase shifter fabricated on quartz substrate. Five phase shifters diced as a chip are mounted onto a carrier for testing as shown in Fig.58.



**Figure 58 Photograph of analog DMTL phase shifter mounted on a test jig**

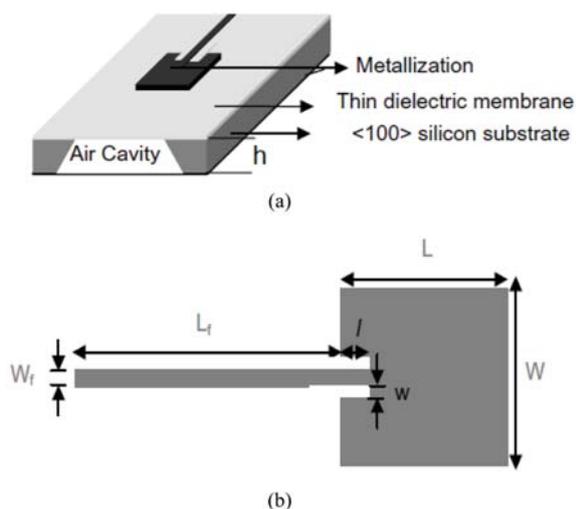
Figure 59 shows the phase shift versus actuation voltage characteristics of the analog DMTL phase shifter at 17 GHz. As observed, the phase shifter gives 300° analog phase shift as actuation voltage is increased from 0-90 V. The maximum insertion loss obtained is 2.6 dB and a return loss better than 20 dB is obtained at 17 GHz.

## 7. Mems antennas

Microstrip antennas are inexpensive low profile antennas suitable for aerospace and mobile applications. These antennas are fabricated on somewhat low dielectric constant ( $\epsilon_r \leq 10$ ) and thick substrates. With the development of monolithic microwave integrated circuit (MMIC) technology, it would be advantageous if antennas can be fabricated on high dielectric constant ( $\epsilon_r \geq 10$ ) substrates such as silicon and gallium arsenide. Microstrip antennas fabricated on high dielectric constant substrates can be easily integrated with MMIC RF front-end circuitry. There are essentially two major factors that limit the performance of an antenna fabricated on high permittivity ( $\epsilon_r = 11.9$ ) silicon substrates. They are (i) excitation of surface waves that results in narrow bandwidth, poor radiation efficiency and degraded radiation patterns, and (ii) losses caused by silicon conductivity. Using silicon-micromachining technology, we can solve the first problem [M.Stotz *et al.*, 1996, Papapolymerou *et al.*, 1998]. Here, the bulk silicon material is removed underneath the patch radiator to synthesize a locally low dielectric constant ( $\epsilon_r = 1$ ) region around the antenna. The second problem is overcome by using a High Resistivity Silicon (HRS) substrate, where the losses due to the substrate conductivity are minimized, thereby

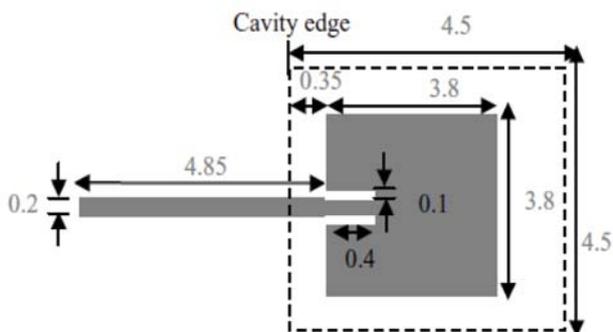
improving the antenna radiation efficiency [Garg *et al.*, 2001].

Details of the work carried out to realize microstrip patch antenna (Fig.59) suspended on thin dielectric membrane using RF sputtering and bulk silicon micromachining are presented here. The issues related to the choice of (i) membrane material and (ii) silicon anisotropic etching solution used are studied.



**Figure 59 (a) Schematic of micromachined antenna suspended on a thin dielectric membrane (b) Conductor pattern**

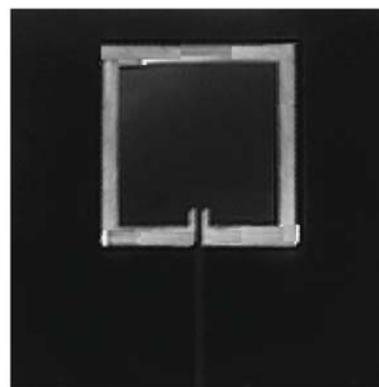
A parametric study of a rectangular patch with various inset lengths  $l$  has been done to obtain an optimized inset length to operate the antenna at frequency of interest. The dimensions of antenna designed to operate at 35 GHz on high resistivity (3000 ohm-cm) silicon substrate are given in Table-VI.



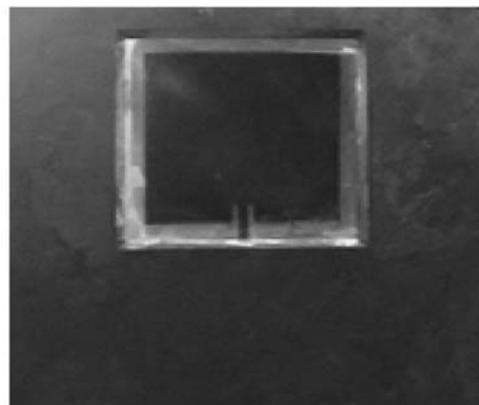
**Figure 60 Typical dimensions of the optimized micromachined antenna.**

**Tale 6: Dimensions of the microstrip antenna on micromachined substrate**

Functional Parameter	Value ( $\mu\text{m}$ )
Dimension of patch, $L \times W$ ( $\text{mm}^2$ )	3.8 $\times$ 3.8
Lateral dimension of cavity ( $\text{mm}^2$ ) in top-plane	4.5 $\times$ 4.5
Lateral dimension of cavity ( $\text{mm}^2$ ) in bottom-plane	4.88 $\times$ 4.88
Length of inset line section $l$ (mm)	0.4
Width of inset slot line section $w$ (mm)	0.1
Length of feed line $L_f$ (mm)	4.85
Width of feed line $W_f$ (mm)	0.2
Thickness of silicon dioxide layer ( $\mu\text{m}$ )	2
Thickness of HRS silicon substrate (mm)	0.27



(a)



(b)

**Figure.61 Photograph of the microstrip antenna on micromachined substrate (a) Top view showing the conductor pattern (b) Bottom view showing the micromachined cavity.**

The antenna structure was next analyzed and optimized using the finite-element method (FEM)-based software package, Agilent High Frequency Structure Simulator. The final dimensions of the patch antenna including the cavity are shown in Fig. 60. This antenna was then fabricated with the process steps used in conventional IC fabrication. A photograph of the fabricated antenna is shown in Fig.61.

For testing, the fabricated antenna was mounted on a test jig as shown in Fig. 62 and excited using a K-connector (Tensolite model no. 230CCSF) to microstrip transition. The center frequency and bandwidth were obtained from reflection measurements. The return loss was measured on a Vector Network Analyzer (VNA) (Rhodes and Schwarz, Model ZVK-1127.8651.60) that was calibrated from 32-38 GHz using the TOSM standards. The measured and simulated return loss characteristics and VSWR of the micromachined antenna are plotted in Figs. 63(a)-(b), respectively. As observed, the simulated and measured data agree well. The operating frequency obtained was 35 GHz and the -10 dB return loss bandwidth  $\sim 1.0$  GHz. The measured impedance bandwidth for  $VSWR \leq 2$  is 3.14%.

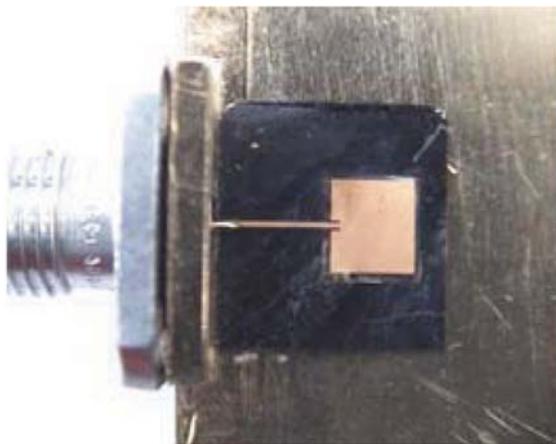


Figure.62 Photograph of the fabricated inset fed microstrip antenna on micromachined substrate mounted on the test jig with K-connector launcher

An exhaustive parametric study of the patch antenna shown in Fig. 60 with various inset lengths  $l$  has been performed using the full-wave finite-element method-based HFSS. The purpose of this study was to obtain an optimized inset depth " $l$ " for which  $S_{11}$  is minimum at design frequency.

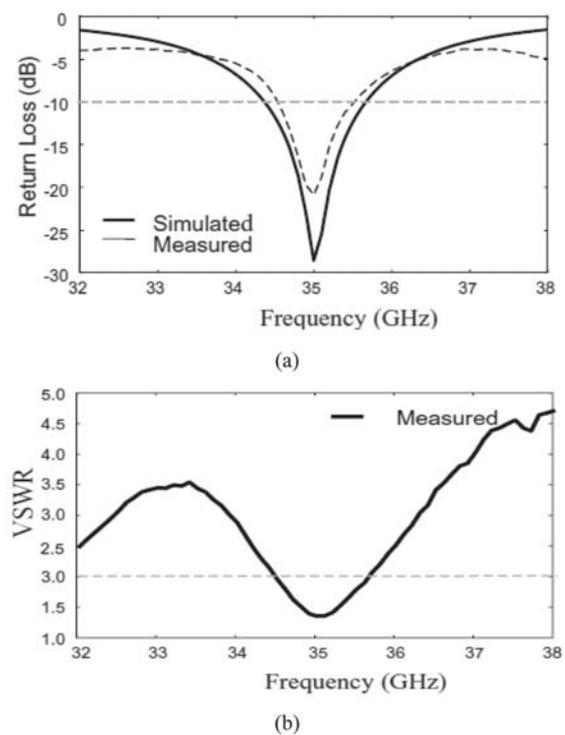


Figure 63 Characteristics of the fabricated inset-fed microstrip antenna on micromachined substrate, (a) Measured and simulated return loss (b) Measured VSWR

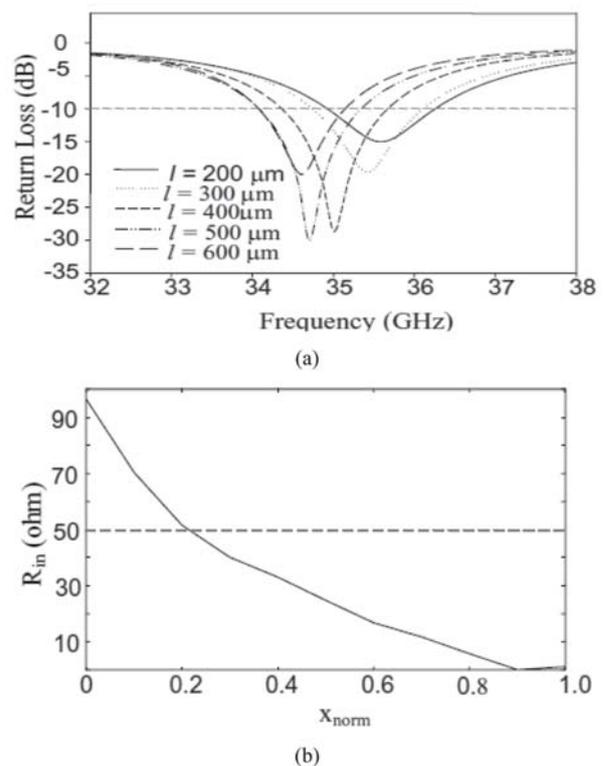
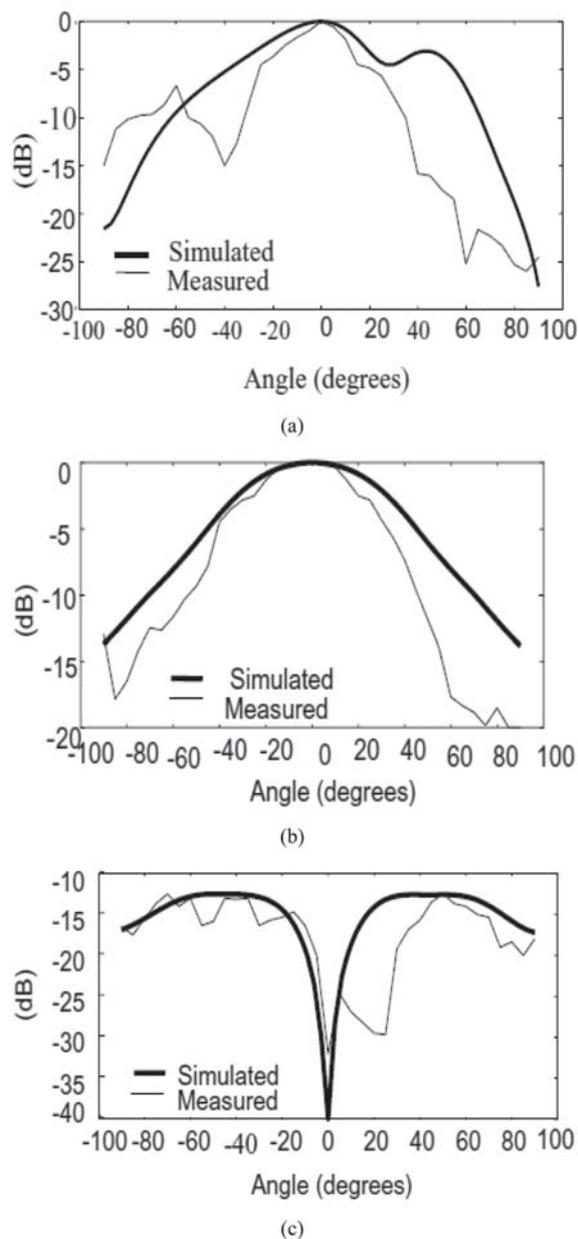


Figure 64 (a) Simulated return loss as a function of frequency for different inset lengths (b) Simulated input resistance  $R_{in}$  as a function of normalized distance  $X_{norm}$ .

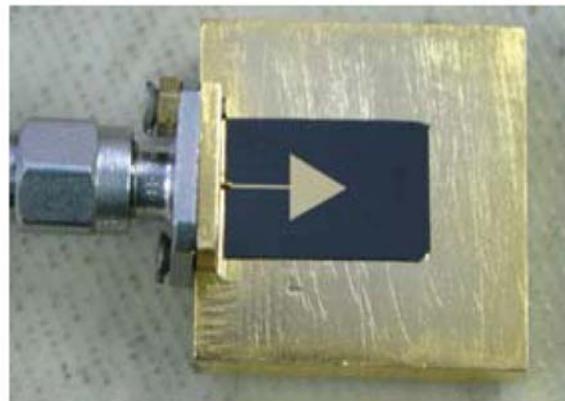


**Figure 65** Radiation patterns of the fabricated antenna on micromachined substrate (a) E-plane, (b) H-plane and (c) cross-polarization

Figure 64(a) shows the return loss characteristics as a function of frequency for different inset lengths and Fig. 64(b) shows the input resistance  $R_{in}$  at the edge of the patch as function of normalized distance  $X_{norm}$  for inset-feed patches with notch width  $w=0.1\text{mm}$ . The normalized feed distance is defined as  $X_{norm} = l / (L/2)$  and the de-embedded length  $L_f = 4.85\text{ mm}$ . From the plots, one can observe that an input match has been achieved at 35 GHz when the inset length is  $400\text{ }\mu\text{m}$ .

Figure.65 shows the measured and simulated E- and H-plane and cross-polarization radiation patterns of the fabricated antenna. As evident from plots, a fairly good agreement between measured and simulated results is observed. The complete antenna structure is realized using post-CMOS- and post-MMIC-compatible metal dielectric deposition techniques.

Triangular patch antennas are reported to provide radiation characteristics similar to those of rectangular patch antennas, but with a smaller physical size. Many researchers have published work on determining the resonant frequency of the equilateral triangular patch antenna excited in the dominant mode [Lee *et al.*, 1988, Guha *et al.*, 2004]. We have designed and fabricated a triangular micromachined antenna on silicon at Ka-band. Photograph of the fabricated antenna mounted on a test jig is shown in Fig.66. Measured results showed the operating frequency as 35.4 GHz and the -10 dB return loss bandwidth  $\sim 1.2\text{ GHz}$ . The

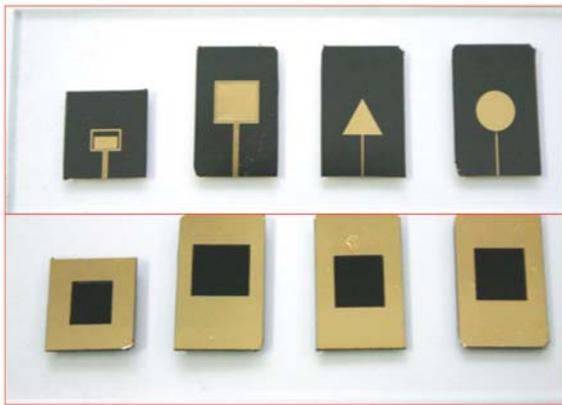


**Figure.66** Photograph of the fabricated triangular microstrip antenna on micromachined substrate mounted on the test jig with K-connector launcher.

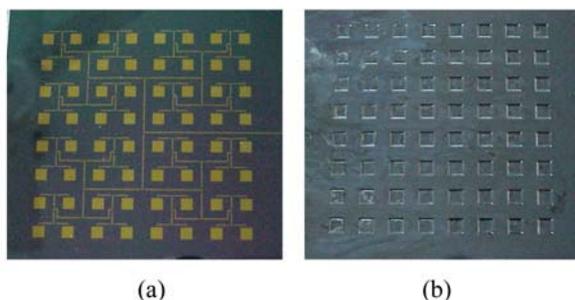
measured impedance bandwidth, for VSWR  $d+ 2$  is 4.23 %.

Several other shapes of the micromachined antennas were also fabricated. These, including coplanar patch antenna, circular patch antenna, slot antenna and the triangular patch antenna have been described earlier. Photographs of these antennas are shown in Fig.67.

Finally, we have realized an 8x8 array antenna on micromachined substrate. A photograph of the array antenna is shown in Fig.68.



**Figure.67** Photograph of different types of patch antennas fabricated on micromachined silicon substrate.



**Figure.68** Photograph of 8x8 array of patch radiators fabricated on micromachined silicon substrate; (a) Top side showing radiating elements connected through power division network, (b) back side showing 64 micromachined cavities

## 8. Mems packaging

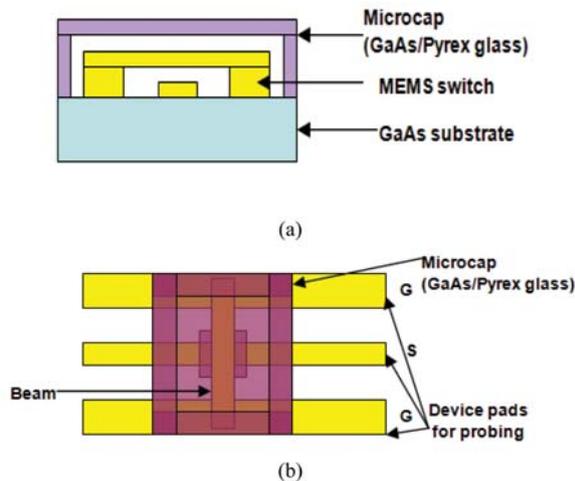
Micro-Electro-Mechanical systems consist of delicate moving parts. These structures are very sensitive to moisture and external environment, and are prone to physical damage during dicing and assembly processes. In order to avoid such damage to the membranes, it is important to package these devices at the wafer level. Various wafer bonding methods have been adopted in practice for wafer-level packaging. The techniques include anodic bonding, thermo-compression bonding, adhesive bonding, etc. [Chao *et al.*, 2004, Seok *et al.*, 2008, Tao *et al.*, 2004, Kim *et al.*, 2008, Lee *et al.*, 2009, Hara *et al.*, 2004, Chiao *et al.*, 2001, Li *et al.*, 2008, Li *et al.*, 2004, Tetelin *et al.*, 2003]. The anodic bonding method works very well for low resistivity substrates like silicon or glass, but not for substrates with high resistivity, like gallium arsenide. Thermo-compression bonding can be used for GaAs-based

RFMEMS but in thermo-compression bonding, specially designed signal vias have to be created for accessing the signal pads of the device. These lead to an increase in insertion loss of the device, losing the primary advantage of MEMS switches [Iannacci *et al.*, 2008, Rotaru *et al.*, 2003, Song *et al.*, 2006, Tian *et al.*, 2008]. The use of adhesive bonding is the most suitable method for GaAs-based RFMEMS. The method proposed here falls in the category of adhesive bonding but is unique in the sense that it does not require signal vias. Moreover, the proposed method is based on fabrication of individual cavities and then aligning and bonding them manually over the MEMS bridge area to protect the beam using an adhesive material. Furthermore, the process does not require expensive wafer bonding equipment. The microcaps are fabricated using GaAs and pyrex glass, with the depth of the cavity covering the beam area varied from 5 to 30 microns to see the effect of vicinity of cap layer on the switch insertion loss and isolation characteristics. It is shown that insertion loss degradation after packaging is less than 0.2 dB, while the isolation of the switch is completely unaffected, in close agreement with the simulation results.

### 8.1 Proposed Concept

Figure 69 illustrates the concept. In this method, the RFMEMS switches and the microcaps are fabricated separately. Both the RF MEMS switches and microcaps were fabricated at the GaAs fab at GAETEC, Hyderabad, India [Saravanan *et al.*, 2009]. CPW lines were also fabricated on the wafer to assess the loss characteristics of the Au electroplated lines as these are the building blocks for the RFMEMS switches [Saravanan *et al.*, 2005]. These CPW lines also serve as the reference to study the insertion loss degradation due to packaging. After fabrication, the microcaps were separated using a high speed ADT 7000 dicing system. Next, the individual caps were inverted and an adhesive material was applied at the interface area. Finally, the caps were carefully aligned covering the beam area, pressed together and cured. The cap structure has been designed in such a way that only the beam gets encapsulated, while leaving the CPW pads accessible for on-wafer probing of the switch. The switch and the cap structures were simulated using an

electromagnetic simulator (CST Microwave studio). Two types of materials were considered for the microcaps, viz., 0.2 mm GaAs and 0.7 mm Pyrex glass. Fabrication details of the microcaps is given in the following section.

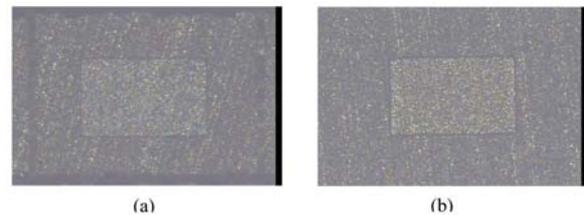


**Figure.69 Proposed micro-packaging concept for GaAs based RFMEMS Shunt switch, (a) Cross section, and (b) Top view**

### 8.1.1 Fabrication of GaAs Microcaps

A mask with patterns consisting of a matrix of  $400\ \mu\text{m} \times 600\ \mu\text{m}$  cavities with a  $200\ \mu\text{m}$ -wide peripheral lining to act as the wall of the cap was prepared. The microcap pattern on the mask was transferred onto  $600\ \mu\text{m}$ -thick semi-insulating GaAs wafers using optical contact lithography. The microcaps were formed by physical etching of GaAs using the reactive ion etching (RIE) process. This process is preferred over the wet chemical etching process for its enhanced selectivity, especially when the etch depths are more than a few microns. A  $6\text{--}7\ \mu\text{m}$ -thick layer of OiR 35 photoresist (PR) was coated on the wafers to act as an etch stop layer during the RIE process. The wafers were subjected to  $\text{O}_2$  plasma cleaning for 2 minutes to ensure good pattern opening. The wafers with the developed pattern were then hard-baked at  $120^\circ\text{C}$  for 30 minutes to harden the PR. Different etch times were used to achieve various etch depths of  $5\text{--}20\ \mu\text{m}$ . After the etching process, the hardened PR was removed by ashing in  $\text{O}_2$  plasma and subsequently in acetone. Different cavity depths in the range of  $5\text{--}20\ \mu\text{m}$  have been fabricated as shown in Fig. 70. The depths of the etched microcaps were then measured using a Dektak surface profiler. All the

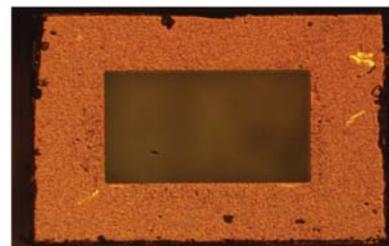
wafers were then thinned down from the substrate side to  $200\ \mu\text{m}$  by lapping. The etched microcaps were then diced.



**Figure 70 Microcap cavities fabricated on  $200\ \mu\text{m}$ -thick GaAs substrate with depths of  $5\ \mu\text{m}$  and  $20\ \mu\text{m}$**

### 8.1.2 Fabrication of glass microcaps

Microcaps were also fabricated in pyrex glass of  $0.7\ \text{mm}$  thickness. As the PR can get damaged by the etchant used for glass etching, a metallic mask was formed on the wafers by depositing a stack of Cr ( $300\ \text{\AA}$ ) and Au ( $1000\ \text{\AA}$ ). The Au layer was further thickened by an additional  $1.8\ \mu\text{m}$  by electroplating. The Microcap pattern was formed on the glass wafers by photolithography followed by metal etching. After metal mask formation, the glass wafers were etched in a cold solution of  $\text{HF}+\text{HNO}_3$  in water in a ratio of  $1:3:7$ . The etch rate was optimized to be around  $1\ \mu\text{m}/\text{min}$  and the samples were etched for different etching times of  $5\text{--}20$  minutes, resulting in cap depths of  $5\text{--}20\ \mu\text{m}$ . Figure 71 shows the micrograph of a glass Microcap. After etching of cavities, the metal mask was removed by etching the Au and Cr metal layers. After fabrication, the individual glass microcaps were diced.

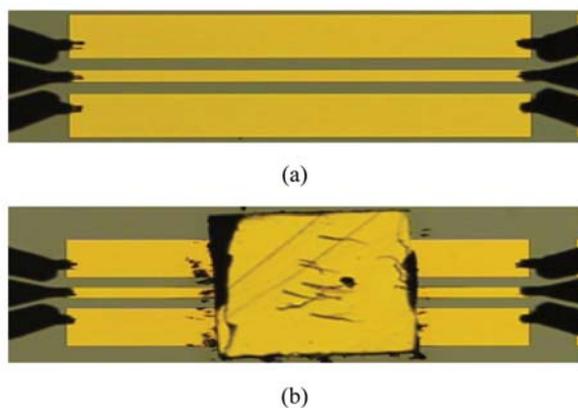


**Figure 71. Microcap cavity fabricated on  $700\ \mu\text{m}$  thick pyrex glass**

### 8.1.3 Cap attachment

For initial verification, the caps were aligned and attached over a  $50\ \Omega$  CPW line as shown in Fig. 72. The insertion loss of a through line was

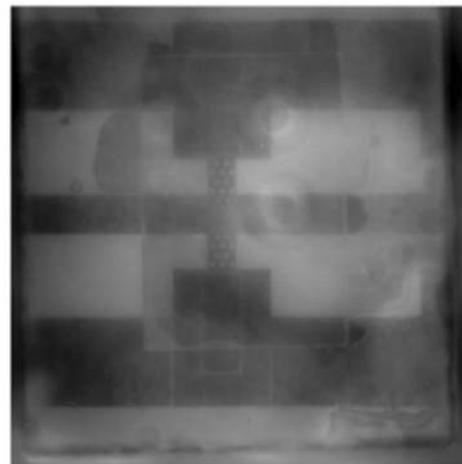
measured prior to and after placing the Microcap. The RFMEMS switches which were to be packaged were measured in the ON- and OFF-states before packaging for reference. The separated microcaps of different depths were picked from different samples (sample # 2, 3, 4 and 7) and were coated with a thin layer of a 2-part non conducting sealant epoxy in the peripheral wall area and manually aligned over the RFMEMS structure. After the alignment, the caps were applied gentle pressure and cured at room temperature. After curing, the packaged RFMEMS switches were measured again in the ON- and OFF-states, and the insertion loss and isolation performance were compared with the results before packaging. Picture of the MEMS structures after packaging with GaAs cap is shown in Fig.73(a). The picture of the GaAs Microcap encapsulated switch was taken through an IR camera as the GaAs Microcap is opaque to visible light. It can be seen that the bridge underneath is intact after the cap attachment. Fig-73(b) shows the micrograph of the Glass Microcap encapsulated switch.



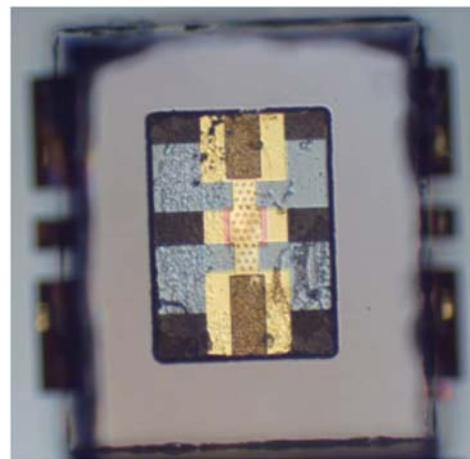
**Figure.72 (a) Reference CPW line and (b) reference CPW line with micro-cap**

## 8.2. Results and discussions

An RFMEMS switch structure with a meandered beam, as shown in Fig. 74, was considered for studying the effect of micro-packaging on its RF performance. Figure 75 shows the simulated effect of micro-packaging with GaAs as the cap material. It can be seen that at a benchmark frequency of 40 GHz, the worst-case simulated insertion loss is 0.32 dB at a cavity depth of 2  $\mu\text{m}$ . The isolation performance is unaltered.

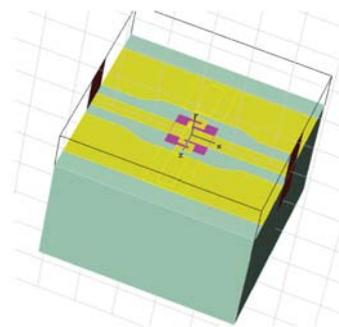


(a)



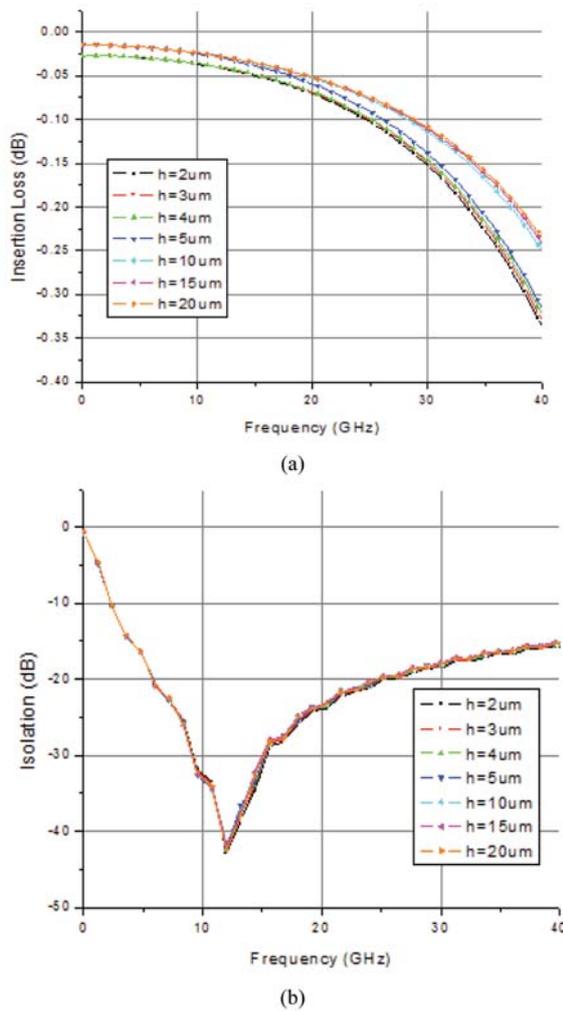
(b)

**Figure.73 (a) IR Micrograph of an RFMEMS switch with GaAs Microcap (b) Micrograph of an RFMEMS switch with the glass Microcap**



**Figure.74 Capacitive RFMEMS shunt switch with Meandered beam**

Figure 76 shows the simulated effect of micro-packaging with pyrex glass as the cap material. The worst-case simulated insertion loss is 0.58 dB at cavity depth of 2  $\mu\text{m}$  at 40 GHz. The isolation performance is unaltered once again. The slight



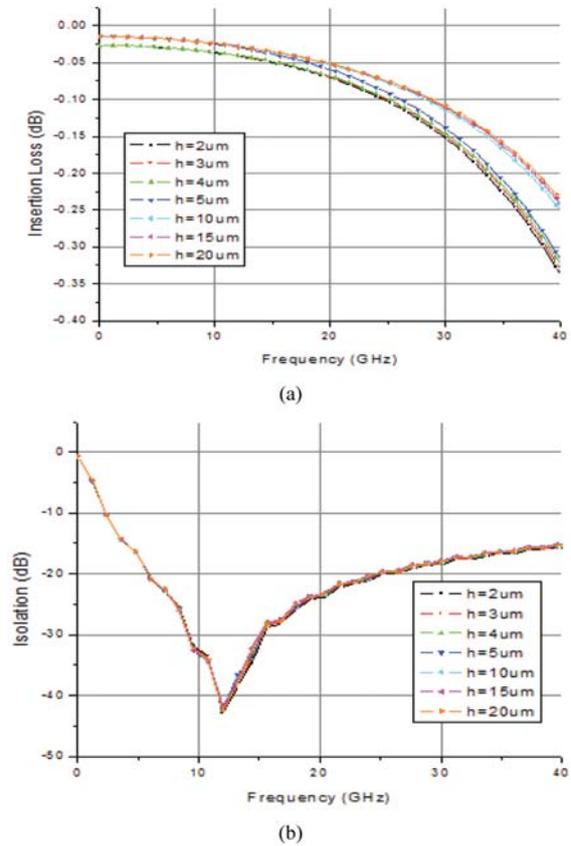
**Figure.75** Effect of Micro-package cavity height on (a) insertion loss and (b) isolation performance of RFMEMS switch for lossy GaAs cap

increase in insertion loss is attributed to higher substrate losses in case of glass.

For initial verification, the fabricated GaAs microcaps were aligned and attached over a 50 Ω CPW line as shown in Fig.72. The insertion loss of a through line was measured prior to and after placing the Microcap. Figure 77 shows the insertion loss of a CPW line without cap, and with GaAs microcaps with depths of 5 and 18 μm. It can be seen that (i) the Microcap has a very small effect on the insertion loss, and (ii) as the cavity height reduces, the insertion loss increases, as predicted by simulation.

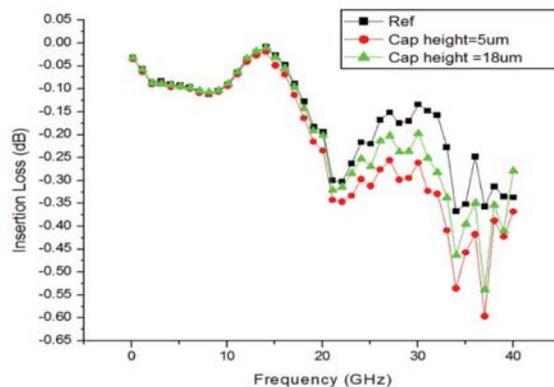
After the verification on the plain CPW line, the GaAs microcaps were attached to the actual MEMS switches. Insertion loss of the switch was

measured before and after cap attachment as shown in Fig.78.



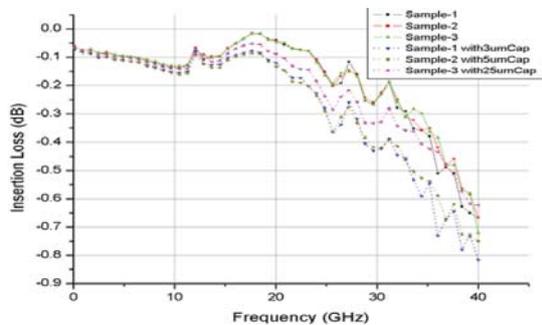
**Figure.76** Simulated effect of Micro-package cavity height on (a) insertion loss and (b) isolation of RFMEMS switch for lossy pyrex glass.

The depths of the representative Microcap samples chosen for attachment were 3 μm, 5 μm and 25 μm. It can be seen that the encapsulation has very little effect (~0.1dB) on insertion loss up



**Figure.77** Effect of micro-cap on the insertion loss of a CPW line

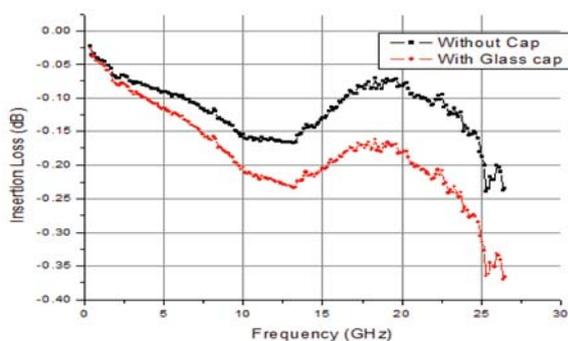
to 40 GHz, confirming the predictions made by simulation. It can also be seen that the loss degradation reduces as the cavity depth increases, as seen in the simulations.



**Figure.78** Measured insertion loss performance of RFMEMS switch without and with GaAs microcaps of various cavity heights

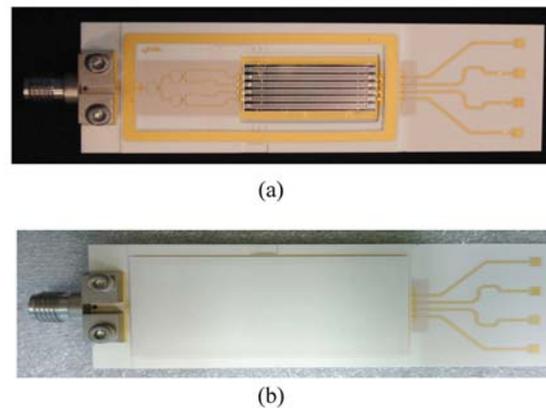
Similarly, the glass microcaps were also attached to the actual MEMS switches. In this case, too, the insertion loss of the switch was measured before and after cap attachment, as shown in Fig.79. It can be seen that the encapsulation has very little effect ( $\sim 0.1$  dB) on insertion loss up to 26.5 GHz.

Besides microcaps, one can also use low temperature co-fired ceramic (LTCC) technology to package a MEMS device and integrate active components and antennas at different layers of the LTCC to form a super component. Figure 80 shows the photograph of a highly integrated MEMS subsystem realized using LTCC technology. It consists of four radiating antennas attached to four MEMS phase shifters fed through power dividers. By changing the bias voltage to the MEMS phase shifter, the beam can be scanned electronically.



**Figure.79** Measured insertion loss performance of RFMEMS switch without and with Glass Microcap

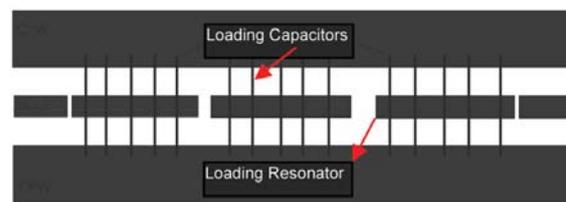
Other RF packaging techniques recently reported can also be explored [Chaturvedi *et al.*, 2013].



**Figure.80** Photographs of 36 GHz LTCC patch antenna array; (a) without and (b) with the LTCC lid.

## 9. Reconfigurable RF Mems Circuits

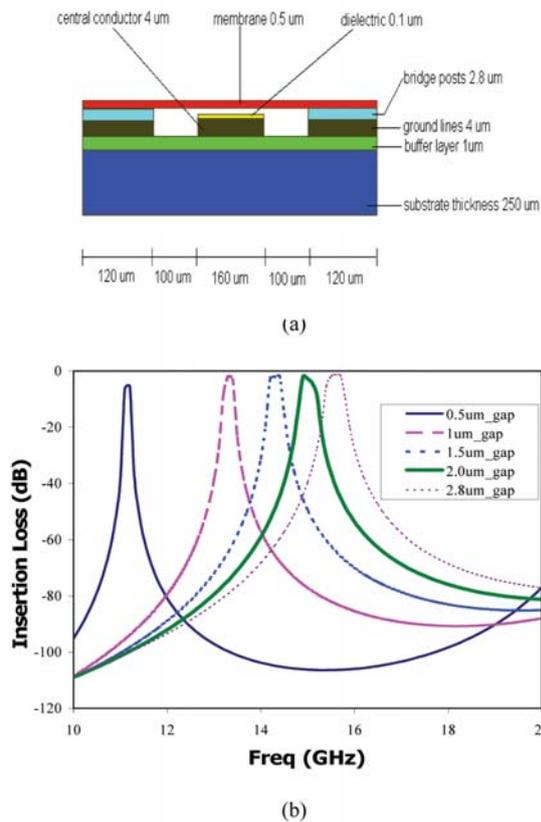
Using variable capacitive bridges and the RF MEMS switches, it is easy to develop a variety of reconfigurable MEMS circuits. Figure 81 shows the layout of the end-coupled filter with multiple bridges loading the resonators.



**Figure.81** Layout of the end-coupled filter with multiple bridges loading the resonators.

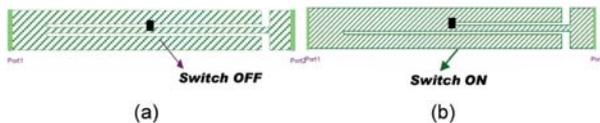
The cross-section of the filter along with its characteristics is shown in Fig. 82. As seen, the filter response can be shifted by applying a control voltage to the loading bridges so as to change the air gap and hence the capacitance.

Figure 82 shows the layout of a band-stop filter on micromachined substrate. This type of band-stop filter consists of two coupled spur line sections. Incorporating an RF switch across one of the slots, as shown in the figure, can make this band-stop filter reconfigurable. Applying a bias voltage to the switch to turn it ON and OFF results in reconfigurable filter characteristics. The filter exhibits stop-band characteristics around 9 GHz, when the switch is in the OFF-state. On the other hand, turning the switch ON results in stop band



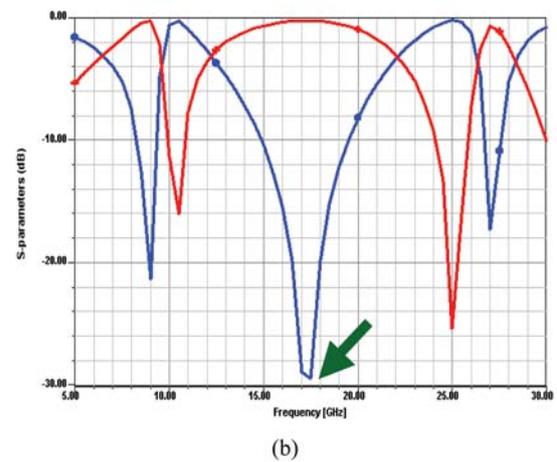
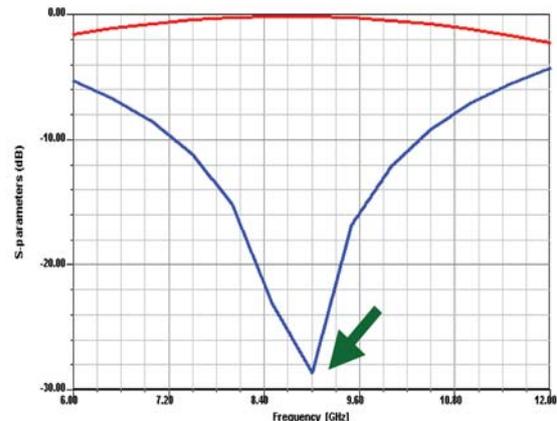
**Figure.81** (a) Cross-section of the end-coupled band pass filter with loading bridges and (b) its response for various air gap heights.

characteristics shifted around 17.5 GHz. Figure 83 shows the response of the filter with switch in the OFF and ON states, respectively. By using multiple switches, the stop band centre frequency can be controlled digitally.

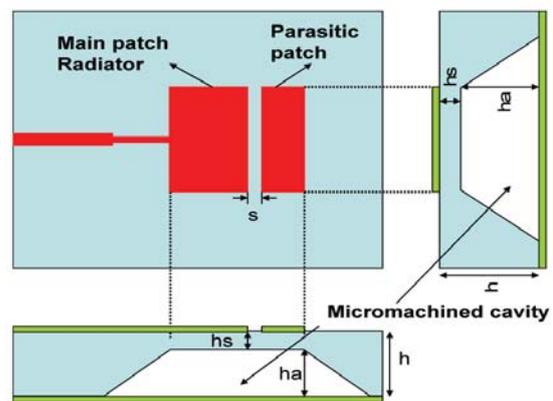


**Figure.82** Layout of the double stub spur line band stop filter on micromachined substrate with RF switch across one of the slots: (a) switch OFF and (b) switch ON

Figure 84 shows a schematic of a micromachined patch antenna suitable for reconfigurability. It consists of a main radiating patch antenna coupled through a small gap 's' to a parasitic patch. By mounting a RF MEMS switch in the gap area, resonance behavior of the antenna can be controlled. The resonance behavior is a strong function of the placement of the switch. One can also use multiple RF MEMS switches in the gap



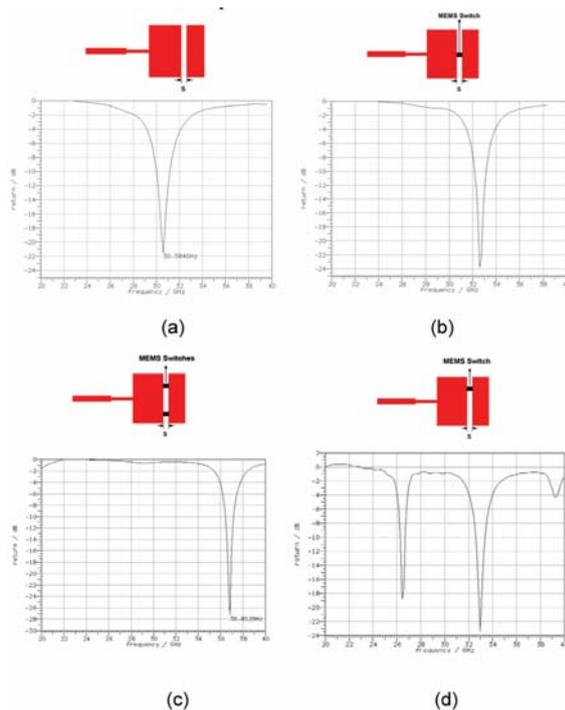
**Figure. 83** Response of the band-stop micromachined filter (a) switch OFF and (b) switch ON



**Figure.84** Schematic of a micromachined patch antenna suitable for reconfigurable resonance

area to reconfigure the resonant frequency of the antenna. Figure.85 show the resonant frequency of the micromachined patch antenna for different switch positions. It is clearly observed that, by

appropriately positioning the switch in the gap 's', resonance characteristics of the antenna can be altered. In practice, one can mount multiple switches and by controlling the bias voltage, reconfigurable resonances can be obtained. By appropriately positioning the switch in Fig.85(d), one can also make the micromachined antenna resonant at two frequencies.



**Figure.85** Resonance characteristics of the micromachined patch antenna (a) switch in OFF position, (b) switch is ON and is placed in the middle, (c) both switches are ON and are symmetrically placed, and (d) switch is ON and is placed asymmetrically

## 10. Conclusion

Recent progress in RF MEMS has been reviewed in this paper from a device perspective. Devices reviewed include switches, tunable capacitors, integrated inductors, filters, phase shifter, antenna, reconfigurable circuits. In addition, different packaging techniques suitable for MEMS devices were also reviewed. Excellent insertion loss and isolation parameters have been observed in RF MEMS switches. Using silicon bulk-micromachining, a wide-band spur-line band-stop filter is described. In addition, development of

micromachined low pass filters using high-impedance, low-impedance design and also stub-line design are presented. A novel topology of a TTD MEMS phase shifter has been found to demonstrate 114.64<sup>0</sup>/dB of FOM from a unit cell on alumina substrate, which is the highest reported FOM at 40 GHz from a unit cell. The proposed device demonstrates differential phase shift of 0<sup>0</sup> - 360<sup>0</sup> upto 40 GHz with minimum actuation voltage of 8.1 V. The design and fabrication of a Ka-band microstrip centre-fed rectangular patch antenna on a suspended 3- $\mu$ m thick silicon-nitride membrane using the silicon bulk-micromachining technique has also been presented. Different types of patch antennas developed on micromachined silicon substrates including 8x8 antenna array have also been discussed. A novel and easy approach for wafer-level encapsulation of GaAs-based RFMEMS switches has been described. Characterization of the packaged switches shows very little deterioration (<0.2 dB at 40 GHz) in switch performance validating the EM simulation approach and viability of implementation of the proposed concept. Finally, utilization of MEMS switches or variable capacitors to develop reconfigurable MEMS circuits including antennas is presented. The intent of this topical review paper is to provide perspectives to newcomers in the field, and empower potential end-users with an overall device picture, current status, and a vision of their ultimate performance capabilities. Future research should be directed towards study of reliability and improvement of power handling capability of the RF MEMS devices, low loss and low-cost packaging techniques, and techniques to reduce switching speed. In addition, integration of CMOS circuits with RF MEMS circuits need to be explored.

## Acknowledgment

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