JISSS, 5(1), pp. 20–30, March–September 2016.

REGULAR PAPER

Identification of hotspots on FPGA using Time to Digital Converter and distributed tiny sensors

Mahantesh P. Mattada[a,*], Sachin M. Magadum[b], Hansraj Guhilot[c]

[a]Department of E&TC, Sanjay Ghodawat Group of Institutions, Kolhapur, India

[b]Department of Electronics RIT, Islampur, India

[c]KC College of Engineering, Thane, India

*Corresponding author: mpmathad@gmail.com; mahant_pm@yahoo.com

Keywords

Time to Digital Converter Vernier TDC Ring oscillator Temperature Sensor FPGA implementation High resolution Low cost

Received: 02-12-2015
Revised: 21-02-2017
Accepted: 01-03-2017

Abstract

Fully digital time-domain temperature sensors are designed and placed at five different positions within FPGA. Five tiny pulse-generators are used as five temperature sensors. Using manual floor-planning four sensors are placed at four different corners and one at center. Single 9-bit Time to Digital Converter is utilized for digital output coding. Vernier Time to Digital Converter with 4 ps picoseconds resolution is presented here. The overall design utilizes 308 logical elements of FPGA, i.e. less than 2% of the total resources. A BIST for testing TDC is also deployed with an area overhead of 110 logical elements. The temperature sensors implemented give nearly 0.25°C temperature resolution and a maximum of ±2 LSB nonlinearity is observed over the range.

1 Introduction

Due to the continuous evolution in VLSI technology, tradeoff between area, power and performance are of much concern. Reducing the chip size creates more problems in thermal management, which in turn affects performance. Inbuilt temperature sensors are necessary for identifying the variation in chip temperature. In our previous work [Sachin *et al*. 2012], this information was used to monitor and controll chip temperature. From last two decades, enough attempts were made in CMOS to design smart temperature sensors with low powerand low area. ADC based smart temperature sensors used earlier suffers from less accuracy and measurement range. Later, TDC based thermal sensors [Sachin *et al*. 2012; Poki *et al*. 2007] tried to overcome these drawbacks. On FPGA, TDC based sensors have additional advantages, viz.: 1. Fully digital 2. Time domain to ease on-chip applications. But they require huge area in both CMOS and FPGA. Also, inherent nonlinearity increases the design complexity. A novel method used in [Jingbo *et al*. 2010] uses Johnson Noise Thermometry, simulated in Matlab, which assured linearity by measuring input noise through a low resolution ADC. However, to extract temperature readings, additional arithmetic hardware is required in integrated sensors, which may increase the complexity and silicon area of the system.

The methodology of conventional temperature sensors is as shown in Figure 1. The single sensing element may be a distributed delay line. ADC/TDC converts the variation in electrical signal (proportional to temperature) into its digital equivalent from, which temperature can be extracted. But this method has inherent

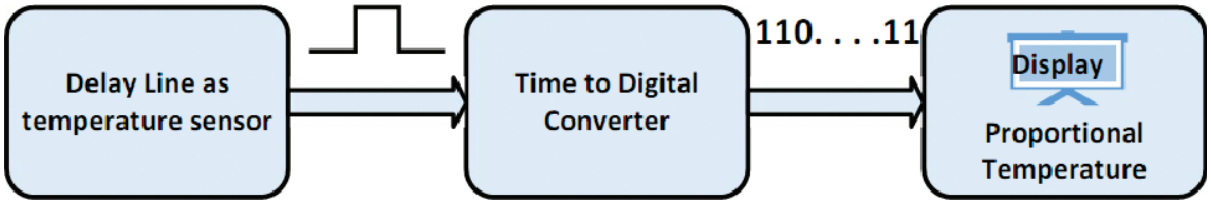

Figure 1. Conventional on-chip temperature sensor.

limitations. Single delay line sensors are unable to identify the part of IC getting heated. This may be because of over usage of a particular IC block or external heat at a corner of IC. If a particular part/component becomes hot, the Single delay line sensor misleads user by showing overall and/or an average increase in IC temperature. This is because of an uneven heat distribution of IC package over the time. Hence, the risk of overheat damage of a particular part/component of IC cannot be identified.

2 Proposed work

This paper presents a novel method of temperature measurement with a high resolution TDC placed and routed on one FPGA, and a number of small sensing elements as temperature sensors are placed on FPGA where critical cores are present. It is essential to monitor and control their temperature for better thermal management of chip; consequently, enhancing the performance of IC. The sensing elements generate a single pulse whose width is proportional to variation in IC temperature. Single Vernier TDC is used to convert pulse width into its digital equivalent. Some key advantages of using Vernier TDC (VTDC) are mentioned here. First, resolution of the thermal sensor depends on resolution of VTDC and not only on size of the sensing element. Second, VTDC uses less number of logic elements compared to other types of TDC. Third, less susceptible to non-linearity as it is induced by self heating. The difference in oscillating periods of two ring oscillator decides resolution of VTDC. Due to change in temperature, periods of ring oscillators will change almost same amount. Hence, time resolution should not be affected. But, VTDC is exaggerated by thermal flux generated at a part of FPGA. In order to keep measuring part, i.e VTDC sovereign for an accurate measurement, a novel testing method is used as discussed in Section 3.

Further, the present work plays an important role in identifying a safe place for the thermally sensitive *critical block*. In case of Network on Chip (NoC) or Multi-core scenario as shown in Figure 2, a job can be assigned to a particular core, which is comparatively cool. Figure 3 shows conceptual diagram of the present work. Four SPGs (Single Pulse Generators) are placed at four corners and one at the centre of FPGA-1. These SPGs act as sensing elements, which is connected to VTDC through a multiplexer. VTDC is manually placed and routed close to IO boundaries of FPGA-2, where there is comparatively less switching activities. Therefore, the cause of temperature is considerably stumpy on TDC and the nonlinearity of TDC during temperature measurement can be evaded.

Testing is an essential task of system design flow to ensure proper functioning. One way to get reliable system is to include testing methodology along with core blocks. Present work includes Built-In-Self-Test (BIST) methodology for testing TDC, thereby assuring an overall reliable performance of the system.

Organization of the paper is as follows. Section 3 explains detail circuits of the implemented work. Section 4 describes simulations

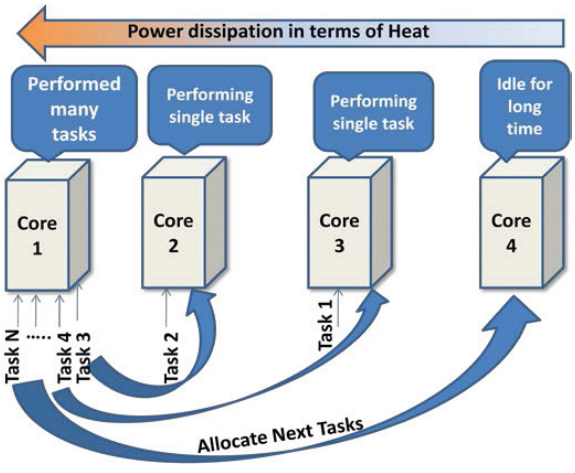

Figure 2. Task allotment in Multi core scenario.

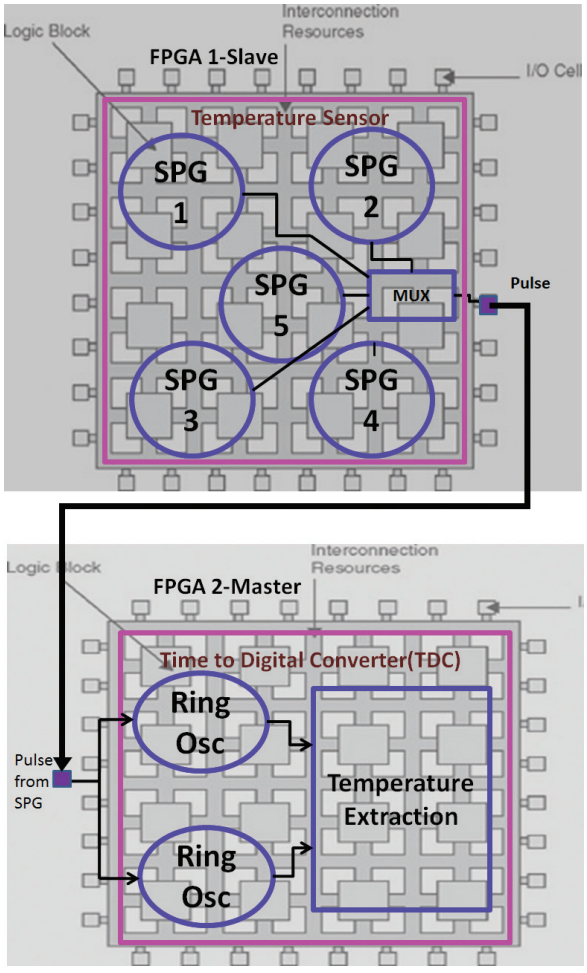

Figure 3. Scenario of the present work shows multiple sensors and single TDC.

and experimental result. Finally, the conclusion is derived in Section 5.

3 System design and implementation

Xilinx's ISE, Isim, PlanAhead software is used for design, simulation and placement. Low cost SPARTAN-3 and SPARTAN-3E FPGAs are used as target devices for implementation of the present work. One can decide how many SPGs are required for a given IC. For convenience, we have used only five SPGs. These SPGs are enabled one at a time and connected to VTDC through a multiplexer. Vernier Time to Digital Converter, which was used in our previous work [Mahantesh & Hansraj, 2013] is retained here with slight modifications.

Overall system implementation is shown in Figure 4. FPGA-1 represents IC under temperature monitoring, where sensors have been deployed. FPGA-2 consists of measurement circuitry, which include TDC and BIST.

3.1 *Single Pulse Generator (SPG)*

Width of the pulse generated by SPG [Mahantesh *et al*. 2015] depends on the number of logic elements used in it. Inherently, it is a delay line with an inverter as a basic element. The proposed design

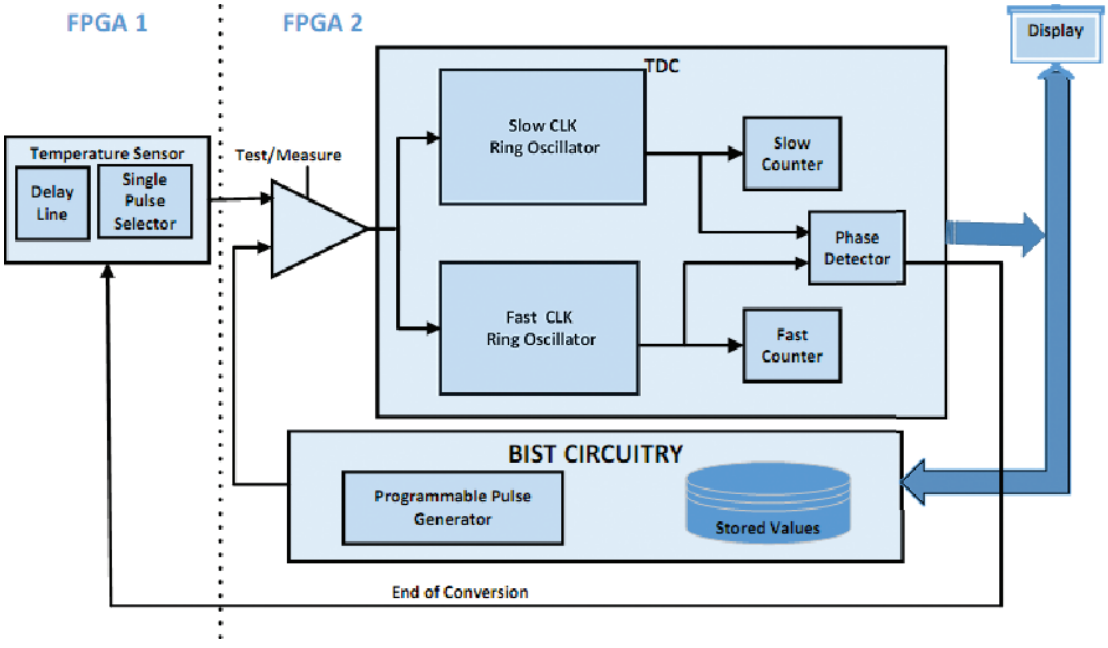

Figure 4. Comprehensive block diagram of the proposed work.

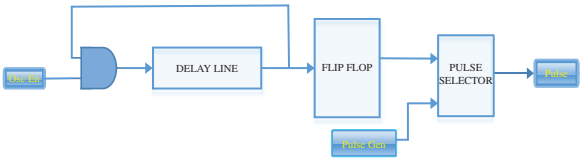

Figure 5. Schematic of Single Pulse Generator.

uses 7 inverters and a flip-flop to generate pulse width of nearly 30.46 ns at room temperature (27°C), which is more sensitive to temperature than SPG introduced in [Mahantesh *et al.* 2015]. Circuit and simulation results are shown in Figures 5 and 6, respectively. Increase in the number of flip-flop increases the pulse width. It is also possible to slightly increase the pulse width by increasing spatial distance between the flip flops, i.e. by varying P&R delay. This can be attained by manual floor-planning using the Plan-Ahead tool [Mahantesh *et al.* 2015]. But SPGs suffer due to setup time and hold time of sequential elements used in each SPG, which produces nonlinearity and adversely affect the pulse generated by SPG, which results in pulse selector output to tristate. The new SPG shown in Figure 5 is comprised of a ring oscillator and a pulse selector. The ring oscillator oscillates at certain frequency depending on the number of elements used in chain at room temperature. As temperature increases, the frequency of oscillations diminish. In other words, output pulse width of the single pulse generator is directly proportional to the rise in temperature. Table 1 shows the number of sensing elements in an SPG and their respective pulse width at room temperature.

The third and fourth column of the Table 1 depicts sensing elements and the resulting pulse width of the modified SPG is shown in Figure 5. For a given number of sensing elements, the pulse width of SPG [Mahantesh *et al*. 2015] is almost equal to pulse width of the proposed SPG. SPG mentioned in [Mahantesh *et al.* 2015] is designed with a complex circuitry with many sequential, combinational logic elements and buffers. Significantly, it obeys the critical timings, viz. setup time and hold time to avoid pulse output to enter into tristate. In contrast, the proposed SPG shown in Figure 5, consists of combinational elements, which are critical on its propagation delay. But this is a vital property for the generation of pulse to measure the temperature.

In principle, width of the pulse generated by SPG is sensitive to temperature. With change in temperature, a pulse of 30 ns may hardly change by few picoseconds. Resolution of the temperature sensor is directly proportional to resolution of TDC. Thus, the resolution of TDC plays an important role in extracting the temperature variation. TDC with sub-picoseconds resolution may not alone serve the purpose. The option is to increase the pulse width by increasing the number of logical elements in sensing line. In [Poki *et al*. 2007] 75 to 4600 logical elements (93% utilization) were made use of to get 0.05°C to 0.07°C resolution. In the previous work [Sachin *et al*. 2012], 107 inverters were used in delay line to attain 0.15°C resolution. SPG shown in Figure 5 with a sequential element and 7 combinational elements is more sensitive to temperature than SPG mentioned in [Mahantesh *et al.* 2015].

Use of the modified SPG [Mahantesh *et al*. 2015] should adhere to the timing constraints of sequential elements for proper pulse generation. SPG shown in Figure 5 generates pulses of different pulse width by channging the number of elements in a chain and more importantly in such SPG time constraints is not an impediment for pulse, since it is comprised of combinational elements as discussed, which is very sensitive to temperature.

Main intention of the present work is to utilize not more than 10% of the total resources of FPGA, thereby providing space for core logic and temperature sensor with good resolution. Figure 7 shows the variation in pulse width generated by SPG, which is dependend on the logic elements in the chain. Some experimental observations with 7, 15, 51 and 65 logic elements within an SPG to

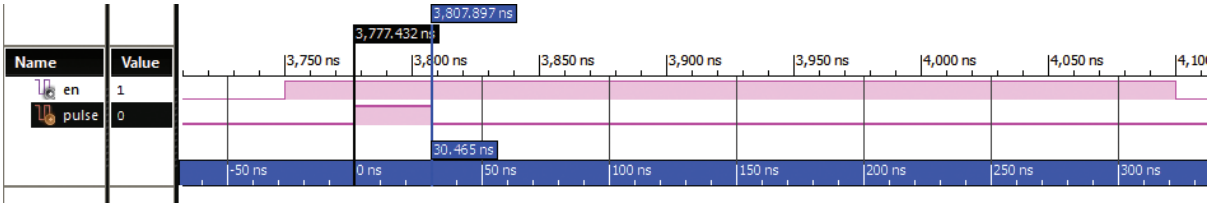

Figure 6. Post Route Simulation of Single Pulse Generator of 7 logic elements and a flipflop.

Table 1. Comparison table of logic elements in different SPGs vs resulting pulse width.

No. of sensing elements in SPG [Mahantesh *et al.* 2015]	Pulse width (ns)	No. of sensing elements in modified SPG [Mahantesh *et al.* 2015]	Pulse width (ns)	No. of sensing elements in proposed SPG	Pulse width (ns)
07	14.5	–	–	7	30.46
15	31.2	15	47.60	15	57.00
21	40.5	21	64.65	21	74.82
35	69.1	35	100.3	35	115.23
51	105.0	51	161.6	51	180.27
65	125.6	65	200.1	65	231.61
81	160.8	81	229.5	81	295.94
101	202.6	101	280.8	101	366.185

sense temperature on FPGA at normal temperature is depicted in Figure 7.

3.2 *Vernier TDC*

Increase in temperature increases delay of the sensing element in SPG, which will reflect in pulse width. The pulse, which is carrying the temperature information should be converted into its digital equivalent. This necessitates a circuit called Time to Digital Converter. The principle of measurement of time interval using Vernier TDC is as shown in Figure 8. There are two controllable oscillators with slight difference in their oscillating periods, and the incremental resolution is

Figure 7. Various widths of pulse generated by SPG on APLAB DSO.

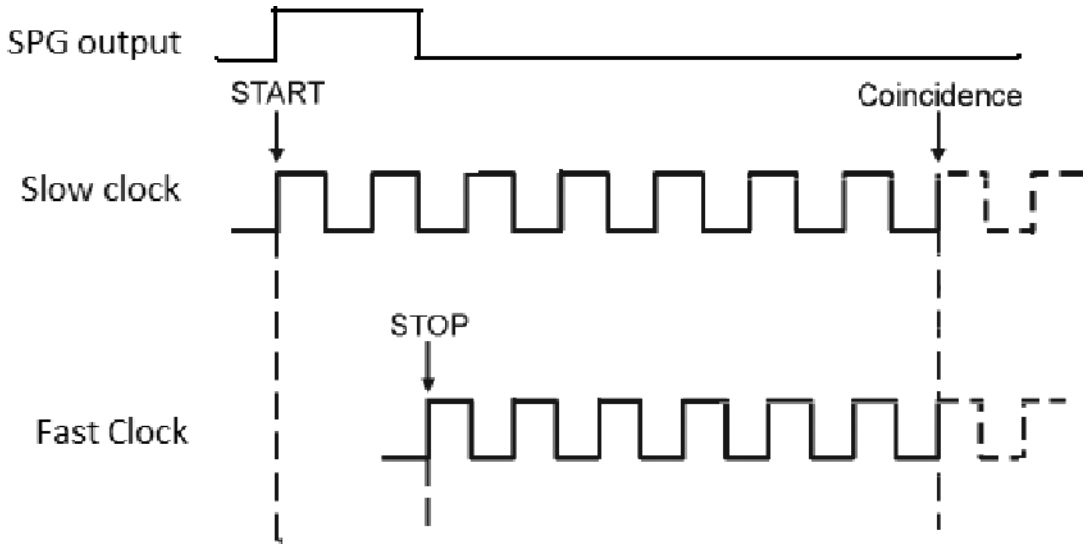

Figure 8. Timing diagram of Vernier TDC.

the disparity between periods of oscillation given by equation 1.

$$T_{resolution} = T_{slow} - T_{fast} \quad (1)$$

The resolution of VTDC is one of the parameter that decides resolution of the temperature sensor. Equation 1 shows that resolution of VTDC will be improved by bringing oscillator periods as close as possible. Many innovative practices are carried out by researchers to get sub-picoseconds resolution. First, an attempt made in [Sachin *et al*. 2008] uses place and route delay to get 40 ps resolution. Second way mentioned in [Poki *et al*. 2010] is to use available PLLs on FPGA to obtain two different frequencies of oscillation and thus, to attain a high resolution of 1.58 ps. Third attempt made in our previous papers [Mahantesh *et al*. 2011; Mahantesh & Hansraj, 2013], show that, oscillation periods can be changed by changing the capacitive load of the ring oscillator.

To meet higher resolution, there should be a fine matching between the two oscillators. The present work proposes a novel way to change the oscillating period. Xilinx's Spartan 3 FPGA has different IO capabilities, viz. LVCMOS 33, 25, 18, GTL, HSTL etc. By assigning different I/O standards for two oscillator output ports, it is possible to vary oscillation period. As depicted in Figure 10, output pin *op* is made as IO standard *LVCMOS18*, where as pin *op2* assigned as *LVCMOS25*. The voltage levels of these two standards are 1.8 V and 2.5 V, respectively. As depicted in Figure 10, post route simulation ensures nearly 6ps resolution. However, pins in that bank will be updated to the same IO standard. One may try with different combinations of IO standard to get further enhanced resolution.

Also, to augment the overall performance with high temperature resolution, a novel testing

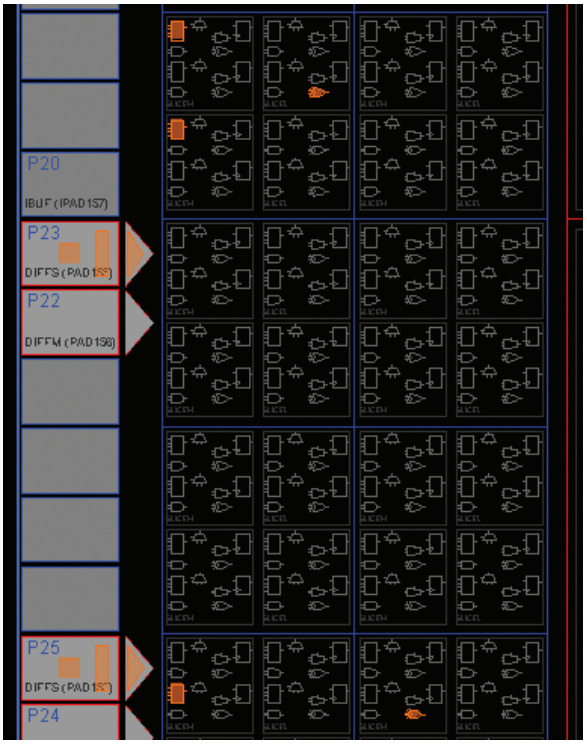

Figure 9. Placement of TDC at edge of FPGA.

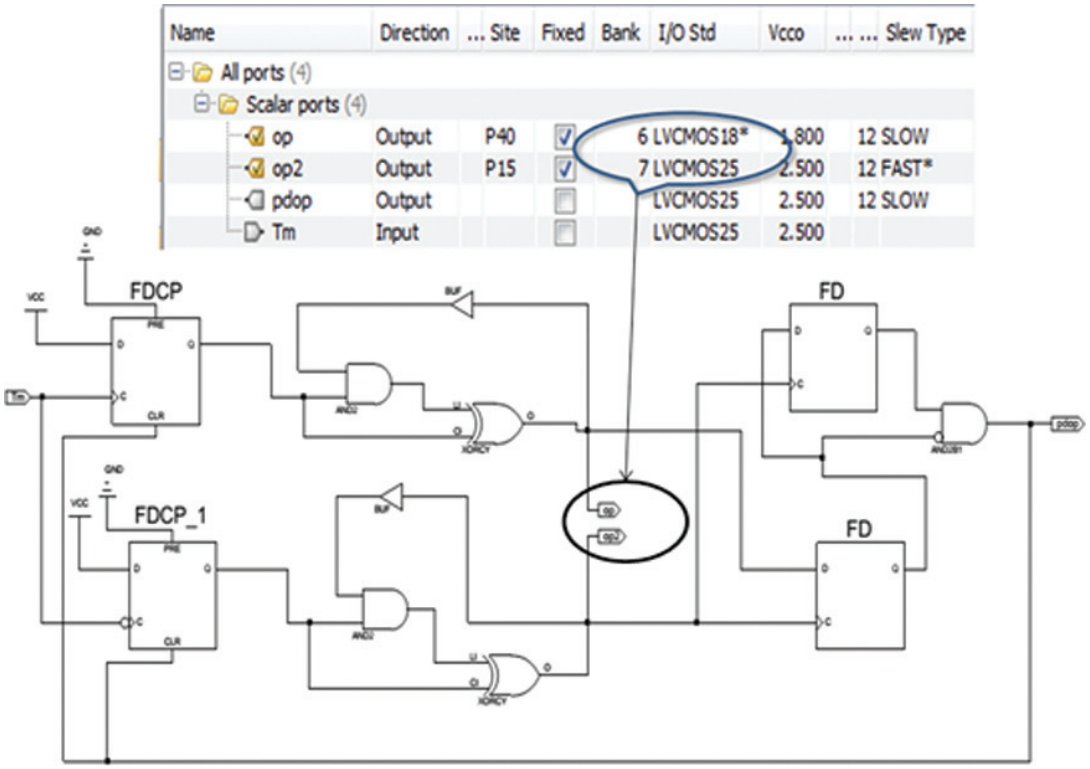

Figure 10. Assignment of different IO standard to VTDC output pins using the Xilinx's PlanAhead tool.

method is presented. This method effectively utilises the amenities of manual place and route of Xilinx tool, i.e. TDC elements are placed and routed on one FPGA, and the Pulse generators are placed on other FPGA in master slave fashion. The master FPGA is responsible for conversion of time into its digital equivalent accurately without consideration of delay due to the system temperature. Components of TDC are placed near the boundaries of FPGA, where the effect of temperature is less due to the fact that system activities are less at CLBs along IO boundaries of FPGA. The placement using the PlanAhead tool is as shown in Figure 9. The function of slave FPGA is to generate a pulse corresponding to the occurrence of the temperature at specific part of FPGA.

Overall system implementation is conceptually described in Figure 3. Using the PlanAhead tool, five modified Single Pulse Generators (SPGs) are placed at different locations of slave FPGA. Thus, time pulse generated by SPG with 7 logic elements is nearly 30.46 ns. This may vary slightly from SPG to SPG, depending on the special disparity in floor planning and P&R delay. A Multiplexer is used to select one SPG output at a time for measurement. A 3-bit counter is used to change the select lines of the multiplexer. Every second, one SPG will be selected to monitor the respective position's temperature. Additional circuits are required to interface seven segment or LCD display. Device utilisation summary generated by the Xilinx' synthesis tool for Spartan 3 (XC3S400PQ208) is as shown in Table 2.

3.3 *BIST*

BIST is specially designed to test TDC operation, where in various pulses of known width are generated by the programmable pulse generator as shown in Figure 12a. The circuit will generate

Table 2. Device utilisation summary.

Logic utilization	Used	Available	Utilization
Number of slices	52	3584	1.45%
Number of slice flip flops	88	7168	1.22%
Number of 4 input LUTs	96	7168	1.34%

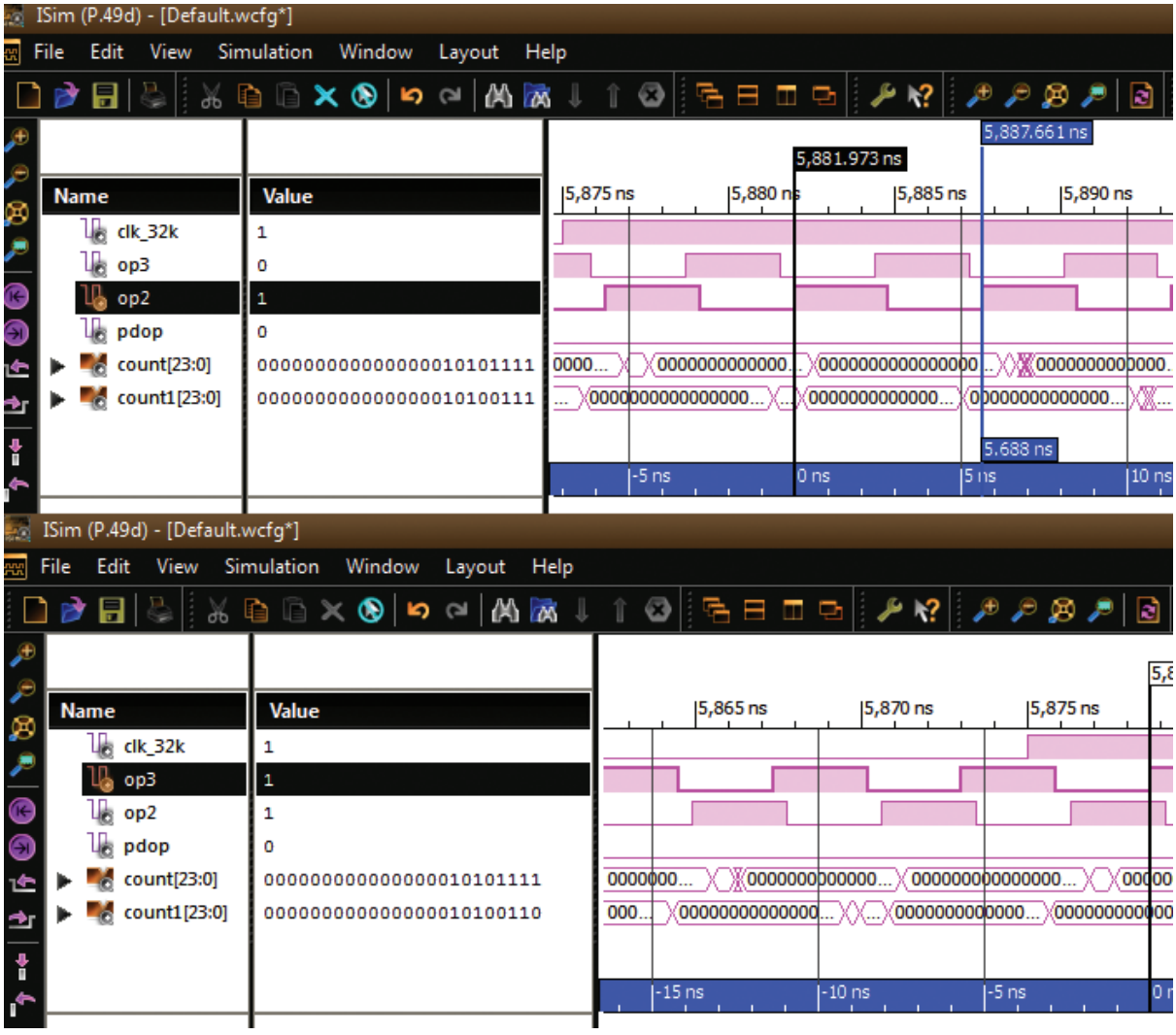

Figure 11. Post route simulation shows 4 ps difference in oscillation periods.

single pulse for each select-line combination. These pulses are then applied sequentially to TDC. The response of TDC is compared with the corresponding digital value stored in the memory. If difference of this comparison goes above the threshold value, BIST will indicate failure. Post-route simulation results of the variable width pulse generator is as shown in Figure 12b.

The deployed testing circuitry needs an additional 110 logical elements. Including this area overhead, less than 2% of the total logic elements are used for overall system. Thus, it provides enough space for core logicand also as an IP it ensures an advantage in silicon real-estate for ASIC implementation. Circuitry to facilitate seven segment display is not considered in the utilization summary.

4 Experimental results

To test the prototyped design, a peltier cooler is mounted on the top of FPGA-1. A temperature sensor is inserted between FPGA and peltier to know the surface temperature. Temperature is varied in steps by changing the peltier supply voltage. The corresponding change in SPG pulse width will be reflected in VTDC counter values. Equation 2 is used to extract the change in width of SPG pulse. Due to tiny size of the sensors, the pulse width changes within a nano second. With 4 ps VTDC resolution, nearly 0.25°C temperature resolution was observed. A plot of temperature verses normalized pulse width is shown in Figure 13. System response is linear up to 80°C and beyond that it saturates slowly. Maximum

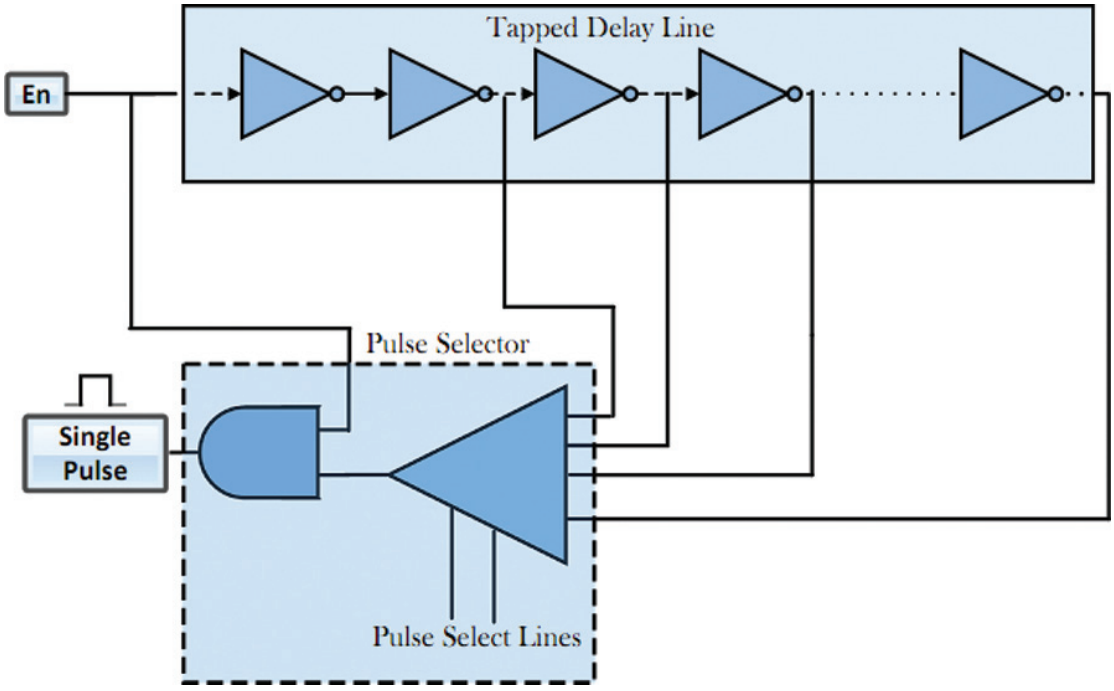

Figure 12a. Variable-width Pulse Generator.

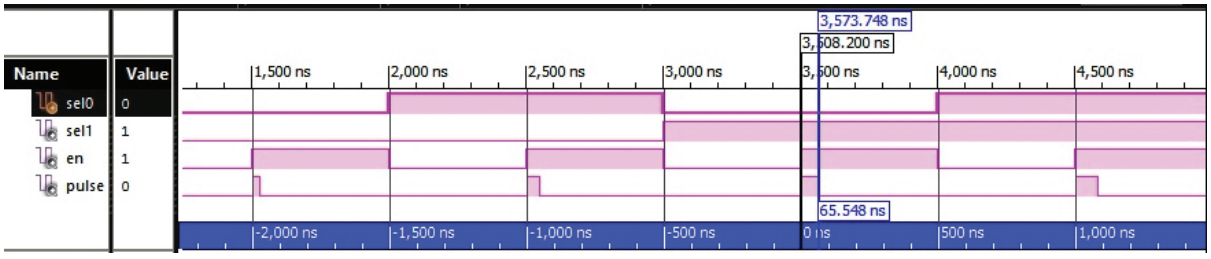

Figure 12b. Post-Route Simulation results of Variable-width Pulse Generator.

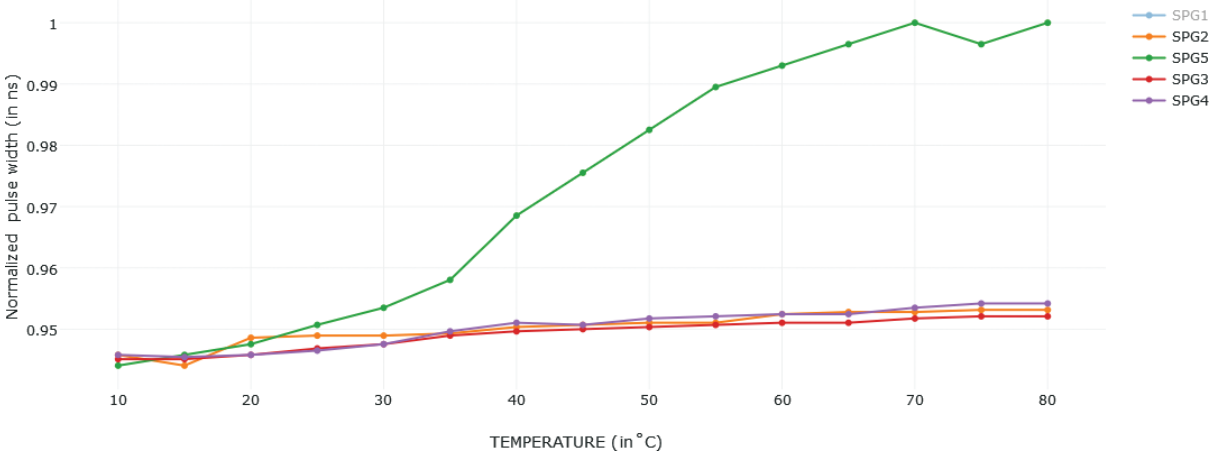

Figure 13. Measured pulse width versus surface temperature.

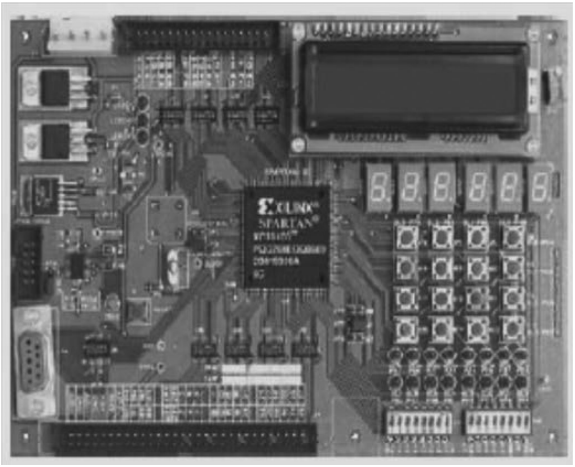

Figure 14. Photograph of Spartan 3 FPGA board.

nonlinearity of the temperature sensor is measured and is found to be ±2 LSB. VTDC nonlinearity with an increase in temperature plays a negative role. Resolution of TDC diminishes at higher temperature. So, post measurement correction is needed at higher temperatures.

$$\text{Pulse width} = (n1-1) * T_{slow} - (n2-1) * T_{fast} \quad (2)$$

By principle, the conversion time of VTDC is going to vary with input range. Also, this dead time increases with an increase in resolution. In the worst case, conversion time of 2 μS for single conversion is ensured from mathematical calculations. It is obvious that VTDC resolution enhancement increases the size of the counters. To operate within 9-bit counter, terminal-count or overflow pin of the counter is also used.

Xilinx's *Xpower Analyzer* is used as the power analysis tool for the present work. By setting node frequencies at Mega Hertz, the dynamic power consumption is obtained from the tool. From a single sensor at 1.15 MHz node frequency, a minimum-measurable dynamic power consumption of 10 μW was recorded. However, it is not necessary to check the temperature with Mega-Hertz frequency.

Figure 14 shows the photograph of FPGA board used for prototyping proposed work. For Master and slave configuration, Two such boards are used seperately.

5 Conclusion

Fully digital time-domain tiny sensors are designed and placed within a low cost FPGA where by an effort was made to identify the hotspot of IC. A novel way to enhance VTDC resolution is presented. With 4 picosenconds TDC resolution as predicted in Figure 11, nearly 0.25°C temperature resolution is assured. Five Sensors, a multiplexer and VTDC together utilize only 308 logical elements. Less than 2% FPGA resource utilization ensures low area and a low power consumption of 10 μW. For a single conversion, maximum dead time is well within 2 μs. A nonlinearity of ±2 LSB is recorded. Temperature range of the sensor is 10–80°C, which makes it suitable for all commercial ranges of ICs. BIST for testing TDC with little area overhead has been successfully deployed.

Acknowledgments

Authors would like to thank, Department of Electronics and Telecommunication, Sanjay Ghodawat group of Institutions and RIT, Islampur for providing necessary hardware boards and tools. This work is supported by Sanjay Ghodawat Institutes, Kolhapur, India. An earlier version of this paper was presented at the 2nd International Symposium on Physics and Technology of Sensors (ISPTS), 2015 and was published in its Proceedings. The web-link and DOI of the same are http://ieeexplore.ieee.org/document/7220119, 10.1109/ISPTS.2015.7220119, respectively.

References

Jingbo, D., Degang, C. and Randall, G. "Sensorless temperature measurement based on ADC input noise measurement." *Proceedings of IEEE NAECON*. 2010.

Mahantesh, P.M. Hansraj, G. and Rajanish K. K. "Area efficient Time to Digital Converter (TDC) architecture with double ring oscillator technique on FPGA for fluorescence measurement application." *Proceedings of IEEE RAICS*. 2011.

Mahantesh, P.M. and Hansraj, G. "Area efficient vernier Time to Digital Converter (TDC) with improved resolution using identical ring oscillators on FPGA." *Proceedings of IEEE ISSS*. 2013.

Mahantesh, P.M. Sachin, M.M. and Hansraj, G. "Identification of hotspots on FPGA using time to digital converter and distributed tiny sensors." *Proceedings of 2nd International Symposium on Physics and Technology of Sensors (ISPTS-2)* (2015).

Poki, C., Mon-Chau, S., Zhi-Yuan, Z., Zi-Fan, Z., and Chun-Yan, C. (2007) "A fully digital time-

domain smart temperature sensor realised with 140 FPGA logic elements." *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I*. **54,** (12) 2661–2668.

Poki, C., Po-Yu, C., Juan-Shan, L., and Yi-Jin, C. (2010) "FPGA vernier digital-to-time converter with 1.58 ps resolution and 59.3 minutes operation range." *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I*. **57,** (6).

Sachin, M., Naveen, K.V. and Hansraj, G. (2012) "Sensor less distributed temperature sensor and control using FPGA." *IJEIT*. **1,** (5) 295–298.

Sachin, S.J., Paul, O'C. and Rejean, F. "FPGA based self calibrating 40 picosecond resolution, wide range time to digital converter." *Proceedings of IEEE Nuclear Science Symposium*. 2008.

Mahantesh P. Mattada was born in Harihar, India in 1986. He received B.E degree in Electronics and Communication, M.Tech degree in VLSI Design and Embedded Systems from VTU, Belagavi, in 2008 and 2011, respectively. He is pursuing PhD at VTU Belgavi.

He is associated with the Department of ETC, Sanjay Ghodawat Institutes, Kolhapur, India. Currently he is working on design, testing and applications of various Time to Digital Converter architectures. His area of interests include CMOS VLSI Design and Digital Design using FPGA.

Sachin M. Magadum was born in Belgaum, Karnataka, India in 1987. He received BE degree in electronics and from Gogte Institute of Technology Belgaum, M.Tech in VLSI Design and Embedded System from KLE College of Engineering and Technology, Belgaum in 2012. He is currently pursuing PhD in VLSI design in VTU Belgaum. His research interests include VLSI thermal management Design of Sensors and development of high resolution TDCs.

Dr. Hansraj Guhilot was born in Haraji, Rajasthan, India in 1958. He received BE degree in electronics from the University Visveswaraiah College of Engineering (UVCE), Bangalore, M.Tech degree in Industrial Electronics from Karnataka Regional Engineering College, Surathakal, India in 1981 and 1985, respectively. He received Ph.D degree in VLSI from Shivaji University, Kolhapur.

Currently he is The Principal of KC college of engineering Thane, Mumbai. He is an expert in power electronics. His patented solution on power processor for metal halide lamps and high frequency electronic ballast. He has published 50+ research papers and was felicitated by the ministry of human resource development, Govt. of India. His areas of interest are smart sensors, agro electronics and mixed mode VLSI design.